SEE1223: Digital Electronics

7 –Semiconductor Memory

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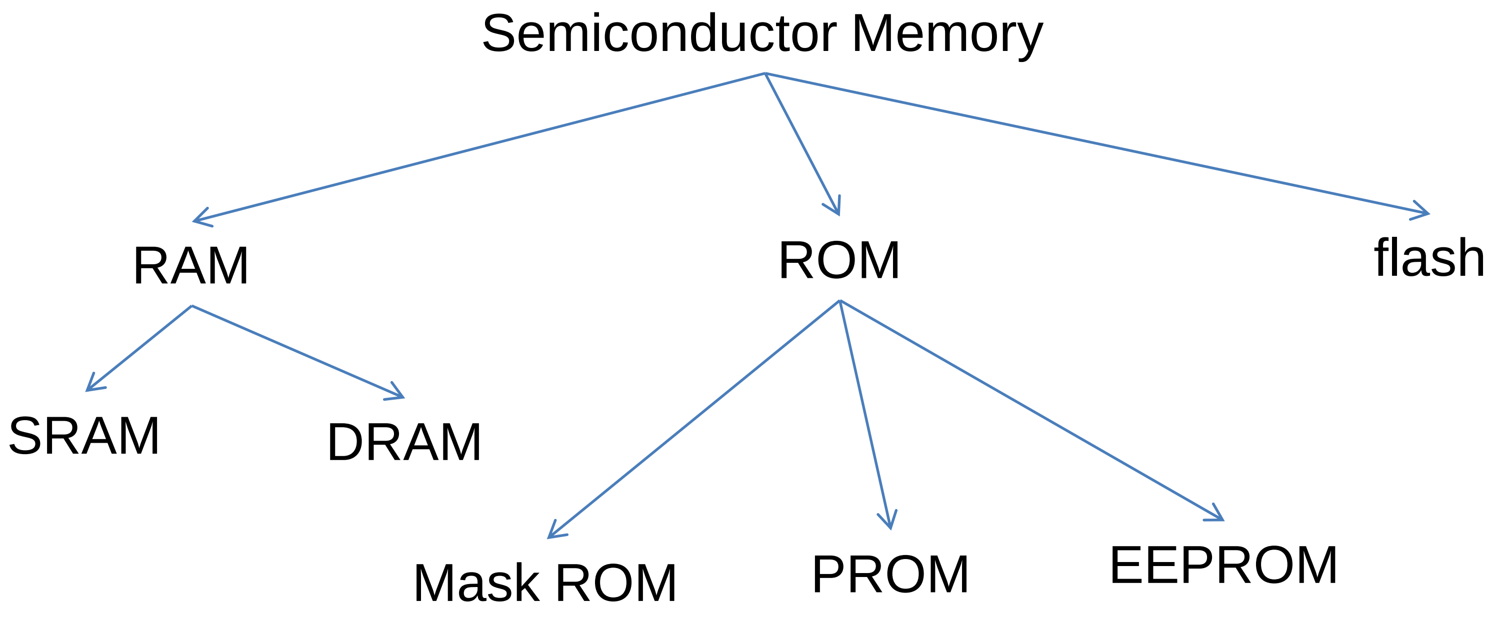
Semiconductor Memory

- Introduction to Semiconductor Memories
- Read Only Memory (ROM)
  - Mask ROM, PROM, EEPROM
  - ROM programming
- Random Access Memory (RAM)
  - SRAM and DRAM
- Flash Memory
- Memory Expansion
  - Capacity and data length expansion
- Memory IC’s

Introduction to Memories

- Semiconductor memories are made from silicon, unlike hard-disk drive memory which are magnetics and optics



Introduction to Memories

- Main difference between memory technologies:
  - RAM
    - Data can be read and written but data stored is *volatile*, i.e. need power to retain data
  - ROM
    - Data can only be read, and the data stored is not volatile, i.e. don’t need power to retain data
  - Flash
    - Data can be read and written, and data stored is not volatile, i.e. don’t need power to retain data

Read Only Memory (ROM)

- ROM is used to store data that never (or rarely) changed
- Data in ROMs are retained even when power is not supplied – main advantage of ROM
- Data in ROMs are typically pre-configured using specialized equipments
- There are three commonly used ROMs: Mask ROM, PROM, and EEPROM

ROM (cont.)

- Mask ROM
  - Data is permanently stored in the memory during the manufacturing process
  - Once the memory array is programmed, it cannot be changed
  - Uses MOS transistor for memory cells
- Programmable ROM (PROM)
  - Uses some type of fusing process to store bits
  - The fusion process is irreversible, one programmed, it cannot be changed
  - Uses MOS transistor with fusible links for memory cells

ROM (cont.)

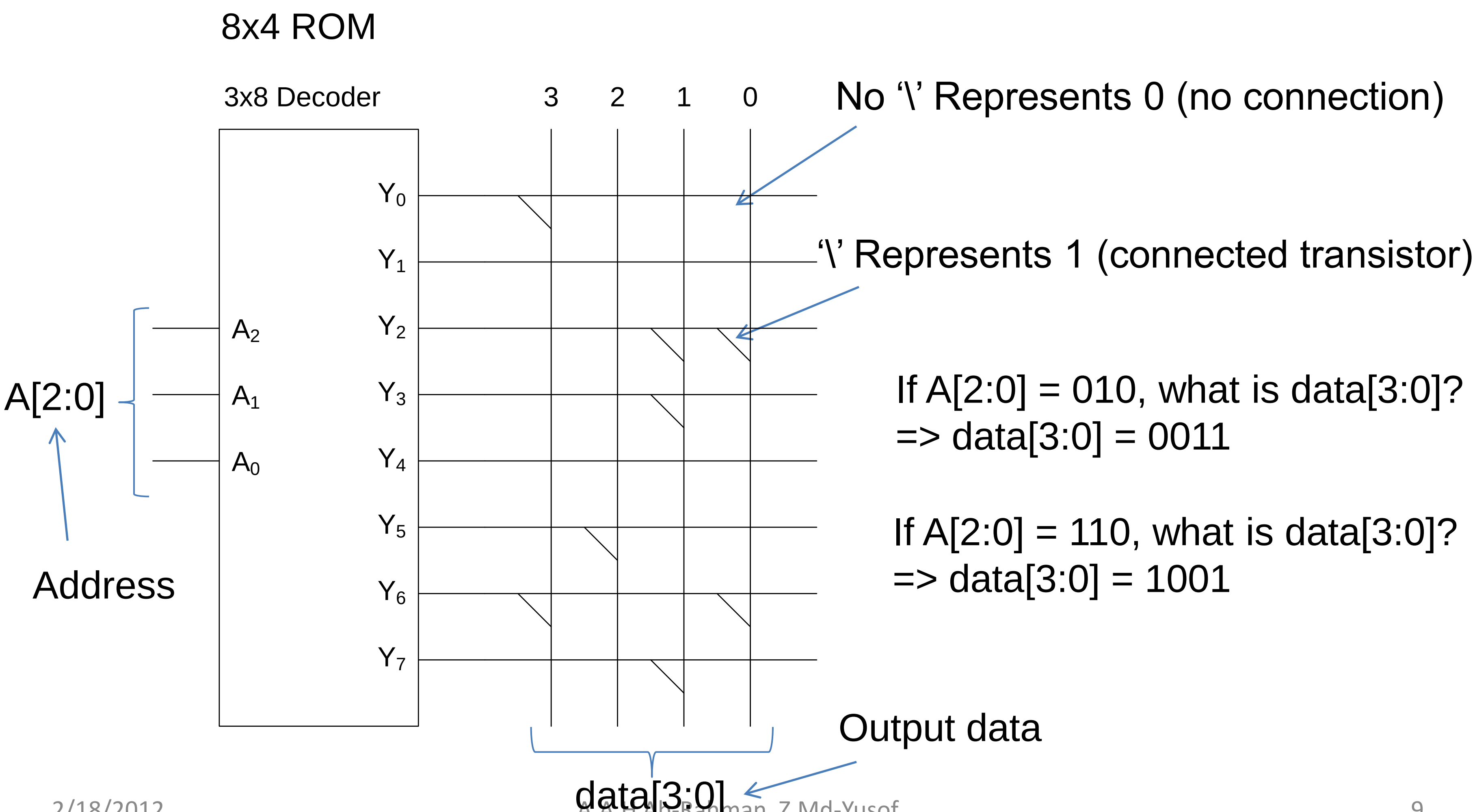
- Electrically Erasable Programmable ROM (EEPROM)
  - Unlike PROM, EEPROM can be reprogrammed if an existing program in the memory array is erased
  - EEPROM is erased and programmed using electrical pulses
  - Therefore, EEPROM can be rapidly programmed and erased in-circuit for reprogramming
  - Uses either floating gate MOS or MNOS transistors for memory cells

ROM Size

- Size of semiconductor memories is represented in bits
- For example, an 8x4 ROM is capable of storing 32 bits
- 8x4 ROM has 3 address lines ($2^3 = 8$) and 4 data lines
- For a 32x8 ROM, how many address line and data lines?
  - Address Line = 5, data line = 8

ROM Programming

- ROM basic construction



If A[2:0] = 010, what is data[3:0]?
=> data[3:0] = 0011

If A[2:0] = 110, what is data[3:0]?
=> data[3:0] = 1001

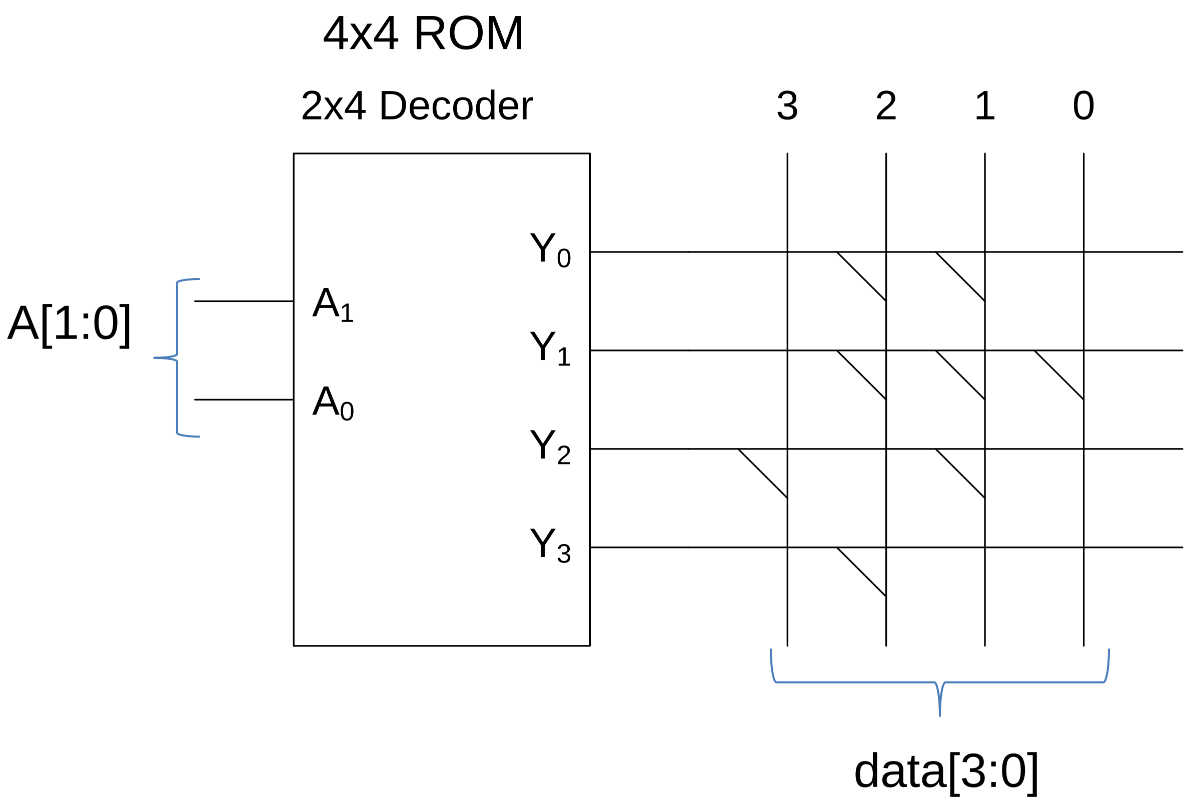
ROM Programming (cont.)

- Design a ROM based on the following truth table

Input Address		Output Data			
A[1]	A[0]	Data[3]	Data[2]	Data[1]	Data[0]
0	0	0	1	1	0
0	1	0	1	1	1
1	0	1	0	1	0
1	1	0	1	0	0

What kind of decoder do we need?
=> 2x4 decoder
What is the size of the ROM?
=> 4x4 ROM

ROM Programming (cont.)

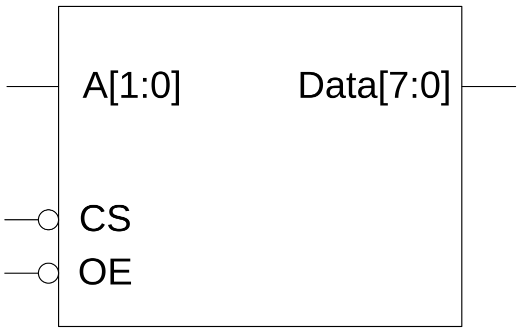


4x4 ROM configured according to the previous truth table

ROM Programming (cont.)

- ROM IC has Chip Select (CS) and Output Enable (OE) pins
  - Output data is valid only when CS = 0 and OE = 0, else data = z (high impedance, i.e. not '0' and not '1')

4x8 ROM



Assume Data[7:0] = 0011 0101
at location A[1:0] = 10

To read the data at location 10,
  Set A_1A_0 = 10
  Set CS = 0, OE = 0
  output Data[7:0] = 0011 0101

If CS = 1 or OE = 1, data [7:0] = zzzz zzzz,
Regardless of the address input A_1A_0

Random Access Memory (RAM)

- RAM is a temporary data storage
- RAM does not retain its stored data when no power is applied
- When a data unit is written into a given address in the RAM, the data unit previously stored at that address is replaced by the new unit
- When a data unit is read at a given address, the data unit that is read remains there
- There are two types of RAM
  - Static RAM (SRAM)
  - Dynamic RAM (DRAM)

The difference is on how each cell is designed

RAM (cont.)

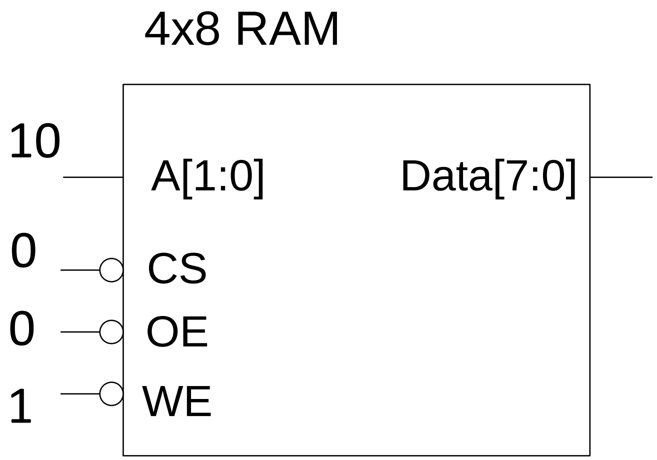
- SRAM vs DRAM
  - SRAM uses a latch to store 1 bit in cell while DRAM uses a capacitor to store 1 bit in a cell
  - Therefore, SRAM is more expensive to implement, i.e. requires more logic gates per cell compared to DRAM
  - Because SRAM uses a latch, it works faster than DRAM that requires the capacitor to be periodically refreshed
  - SRAM is typically implemented in high speed CPU cache memory, while DRAM is implemented in main memory

RAM (cont.)

- How to read from and write to a RAM?
  - Provide the address and data we want to read or write
  - We also need a few enable signals to control when we want to enable the memory, read, and write operation
  - The Chip Select signal (CS) is used to enable the memory
  - The Write Enable signal (WE) is used to enable the write operation
  - The Output Enable signal (OE) is used to enable the read operation

RAM (cont.)

- Read operation example: Read one byte at location A[1:0] = 10 from a 4x8 RAM



Step 1: Supply address A[1:0] = 10 to Read location 10

Step 2: Set CS = 0 to enable the memory

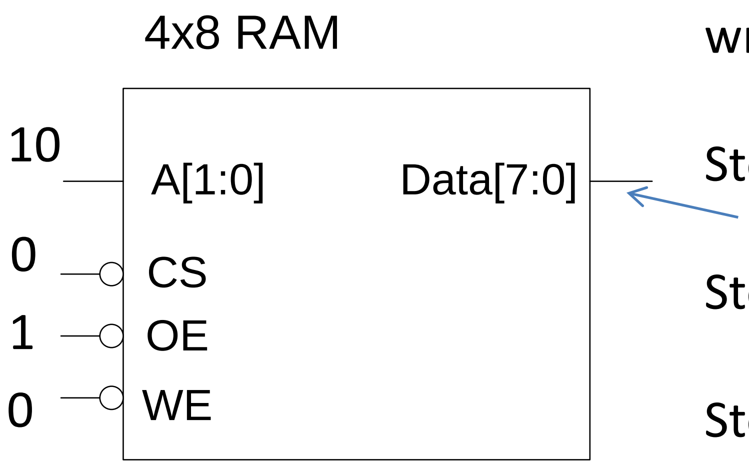
Step 3: Set OE = 0 to enable read

Step 4: Set WE = 1 to disable write

Step 5: Get the data at location 10

RAM (cont.)

- Write operation example: Write one byte at location A[1:0] = 10 from a 4x8 RAM



Step 1: Supply address A[1:0] = 10 to write location 10

Step 2: Supply the Data[7:0] to write
Example: 1010 0111

Step 2: Set CS = 0 to enable the memory

Step 3: Set OE = 1 to disable read

Step 4: Set WE = 0 to enable write

Step 5: data[7:0] is written at location 10

Flash Memory

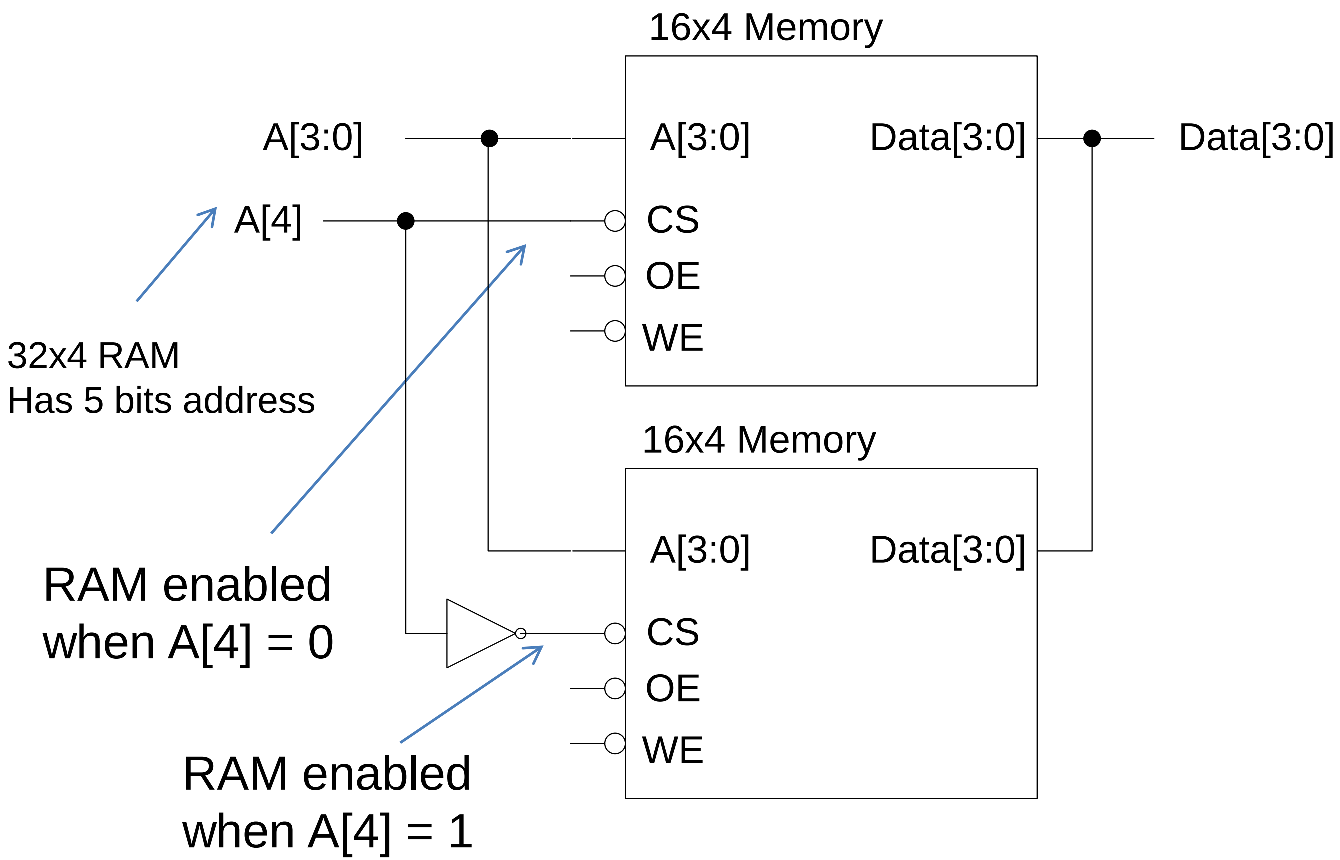
- Flash memory is the closest to the ideal memory:
  - capable of high storage capacity
  - retains data when power off
  - ability to erase and reprogram at will
  - fast operation
  - Cheap
- Flash memory cell is designed using stacked gate MOS transistor (floating gate transistor)

Memory Expansion

- Memory can be expanded on its capacity or data length
  - Capacity expansion example: **16**x4 memory expands to **32**x4 memory
  - Data length expansion example: 16x**4** memory expands to 16x**8** memory

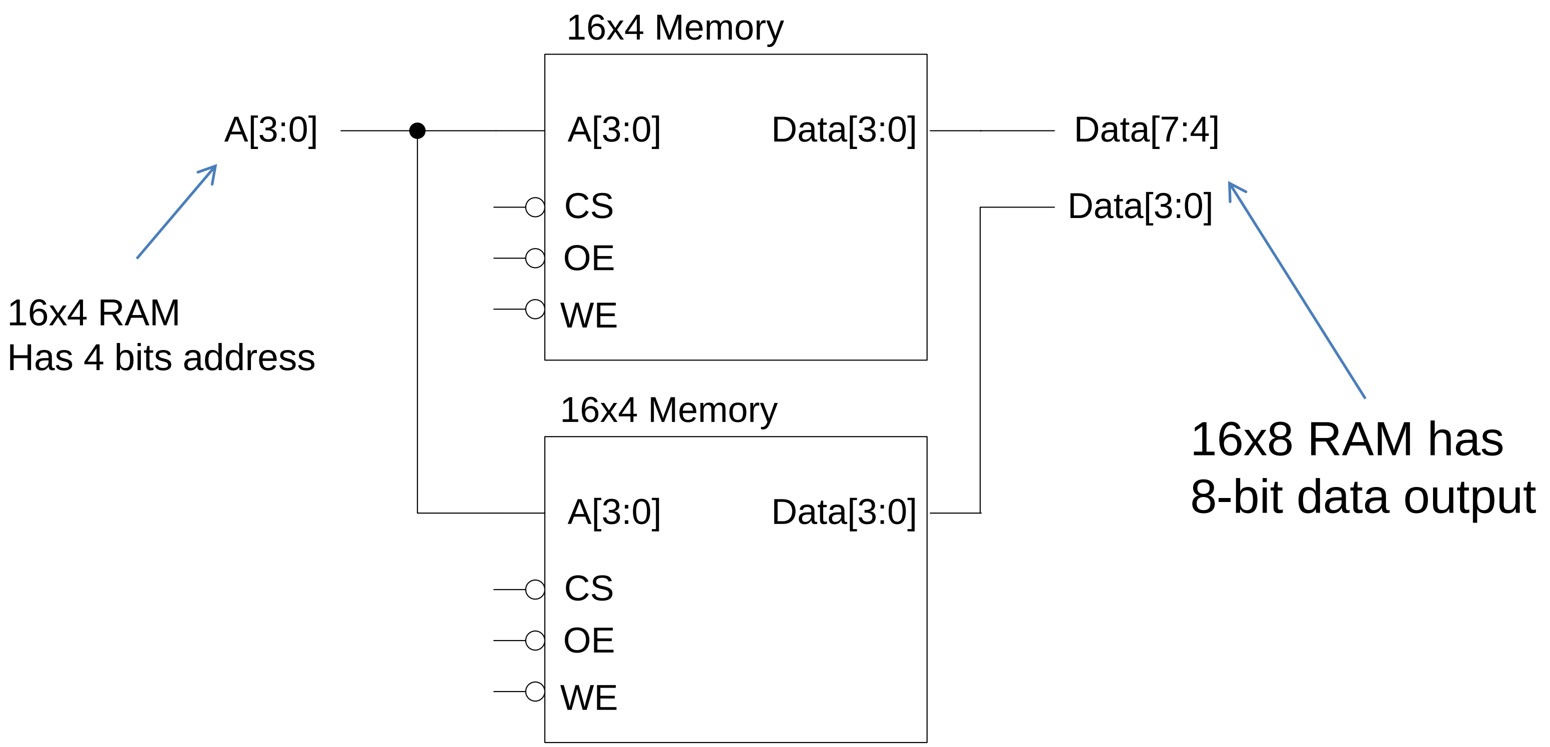
Memory Expansion (cont.)

- Capacity expansion – Use two 16x4 RAM to produce a 32x4 RAM



Memory Expansion (cont.)

- Data length expansion – Use two 16x4 RAM to produce a 16x8 RAM



Memory IC

- 2864 device: 8Kx8 EEPROM – How many address lines and data lines?
  - 13-bit address line, 8-bit data line EEPROM
- 6264 device: 8Kx8 SRAM – How many address lines and data lines?
  - 13-bit address line, 8-bit data line SRAM