

# Counter and Registers

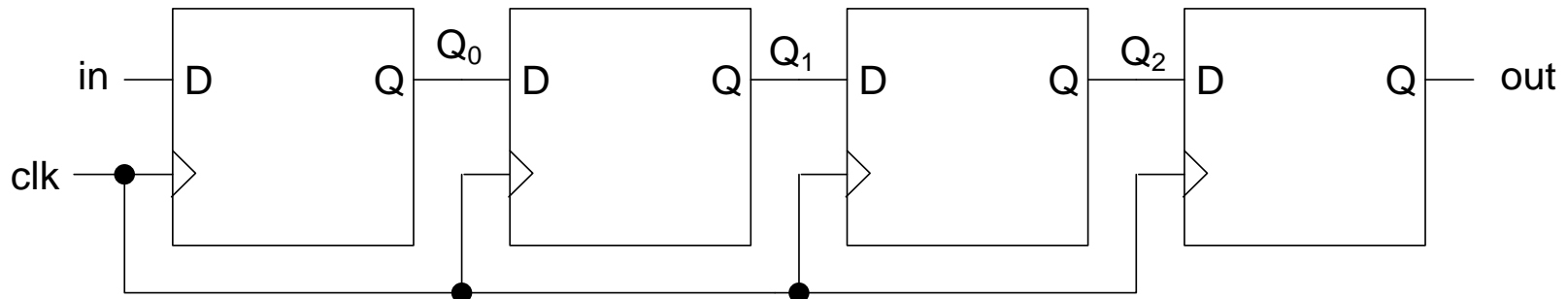
- Counters
  - Asynchronous Counters
  - Synchronous Counters
  - Design of Synchronous Counters
  - 74163 devices
- Registers
  - Shift Registers
    - SISO, SIPO, PISO, PIPO
  - Shift Register Counters
    - Johnson and Ring
  - 74164, 74165, 74194, and 74195 devices

# Shift Registers

- Shift registers are used primarily for storage and data movement
- There are four types of shift registers
  - Serial In Serial Out (SISO)
  - Serial In Parallel Out (SIPO)
  - Parallel In Serial Out (PISO)
  - Parallel In Parallel Out (PIPO)
- All the shift registers are arrays of flip-flops, arranged in certain ways

# Serial In Serial Out (SISO)

- 4-bit SISO shift register
  - Each clock pulse will move an input bit to the next flip-flop



when  $\text{clk} = \uparrow$

$Q_0 \leftarrow \text{in},$

$Q_1 \leftarrow Q_0$

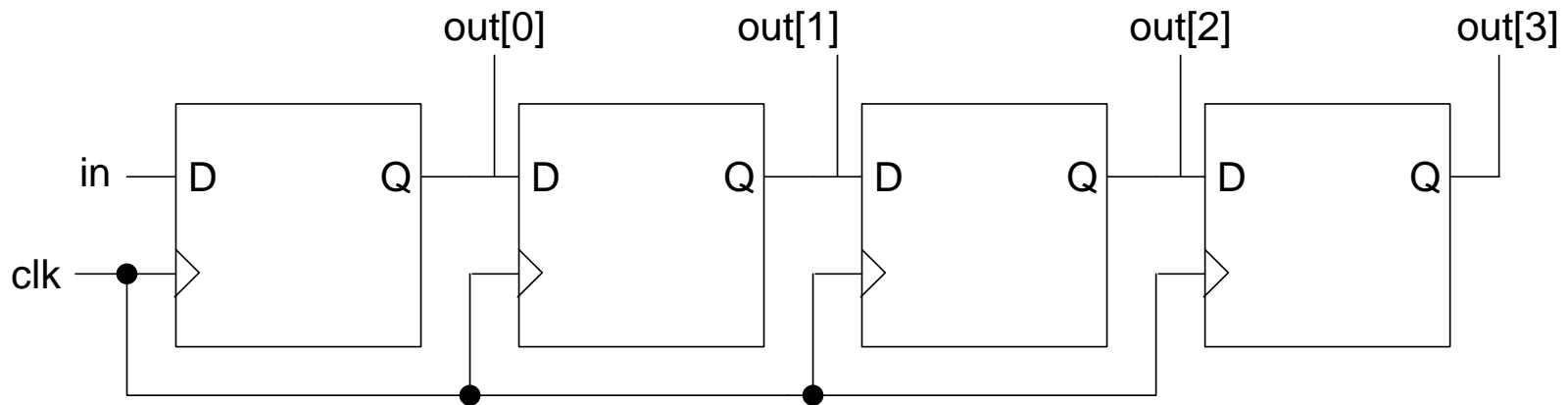
$Q_2 \leftarrow Q_1$

$\text{out} \leftarrow Q_2$

Input is 1-bit *in*, and output is 1-bit *out*

# Serial In Parallel Out (SIPO)

- 4-bit SIPO shift register
  - 1-bit input *in*, and 4-bit output *out[3:0]*



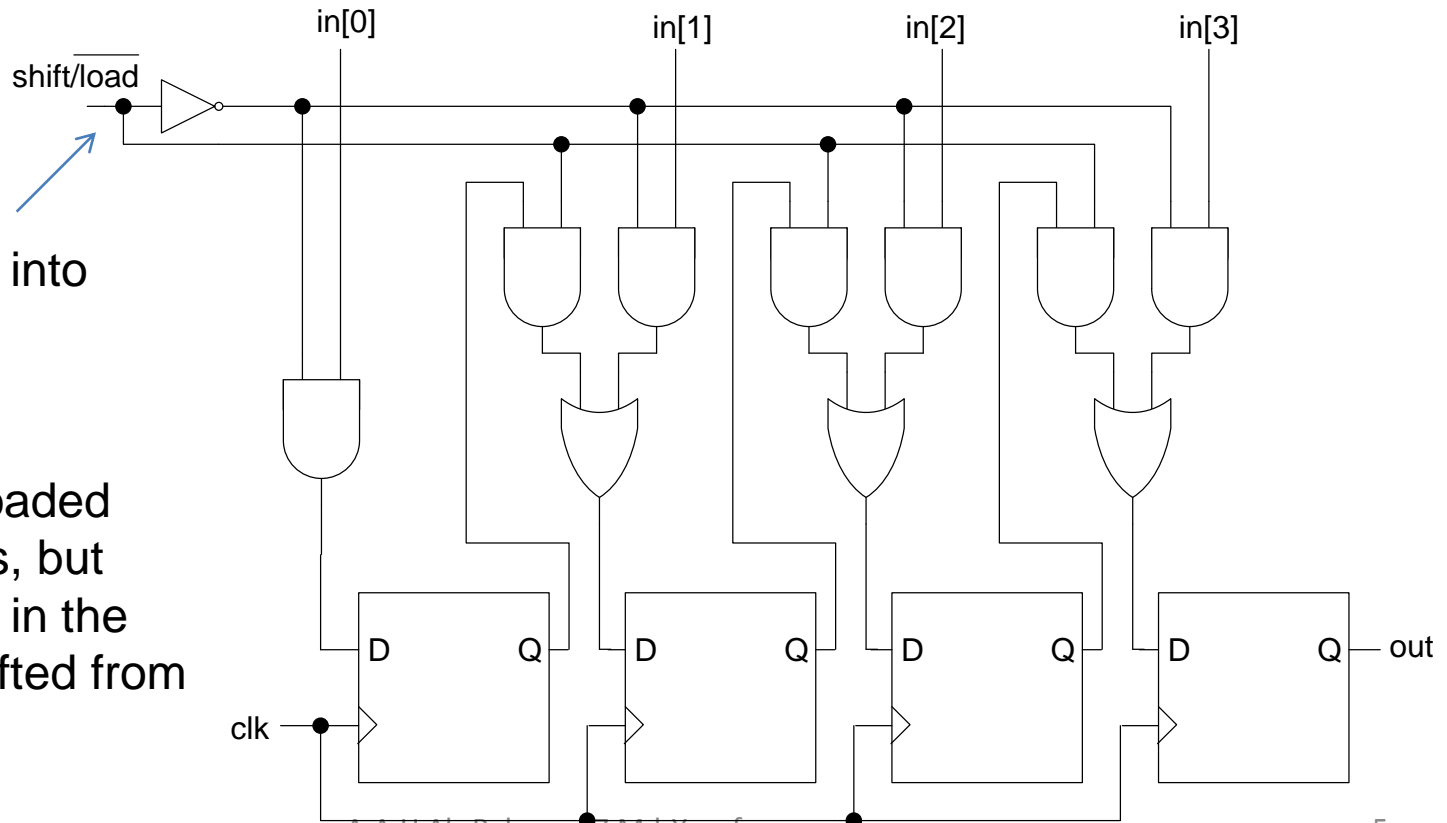
when  $\text{clk} = \uparrow$   
 $\text{out}[0] \leftarrow \text{in}$ ,  
 $\text{out}[1] \leftarrow \text{out}[0]$   
 $\text{out}[2] \leftarrow \text{out}[1]$   
 $\text{out}[3] \leftarrow \text{out}[2]$

# Parallel In Serial Out (PISO)

- 4-bit PISO shift register
  - 4-bit input  $in[3:0]$  and 1-bit output  $out$  with *shift/load* functions

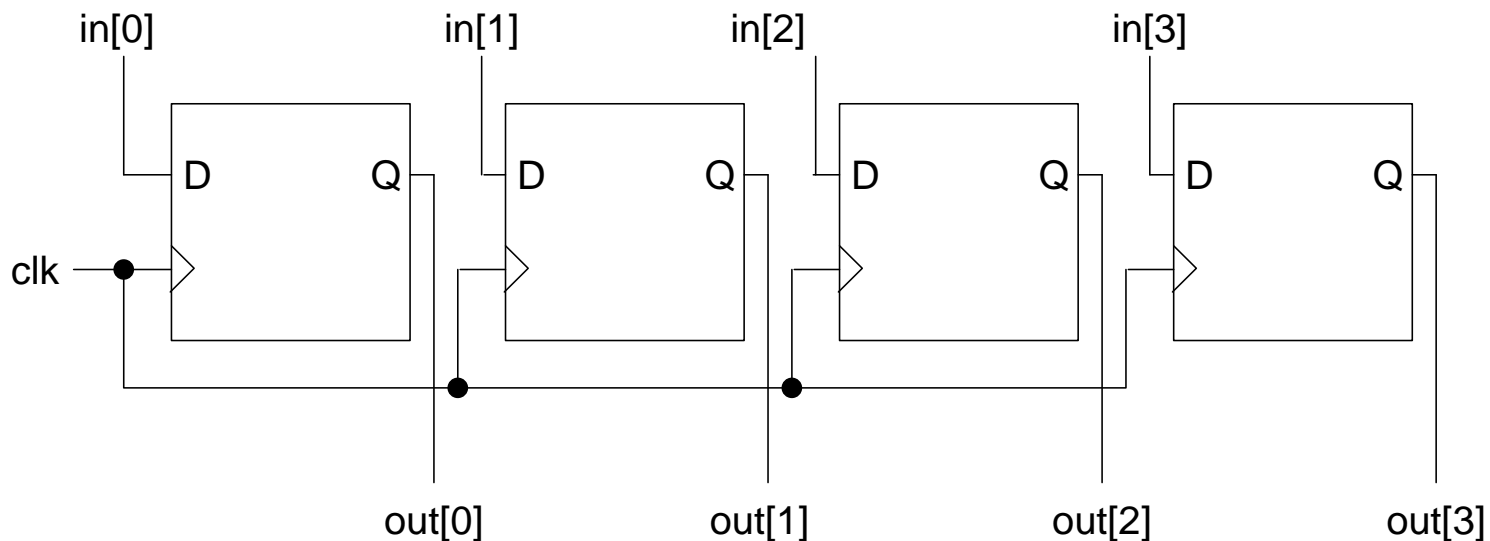
If  $\overline{shift/load} = 0$ ,  
 $in[3:0]$  is loaded into  
 the flip-flops

If  $\overline{shift/load} = 1$ ,  
 $in[3:0]$  is NOT loaded  
 into the flip-flops, but  
 the current data in the  
 flip-flops are shifted from  
 left to right



# Parallel In Parallel Out (PIPO)

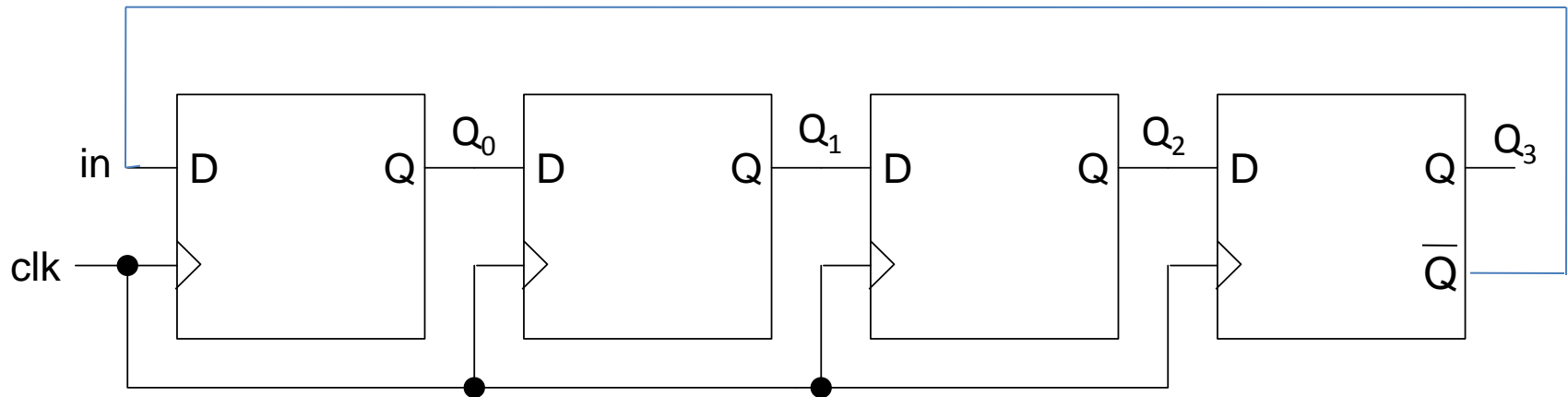
- 4-bit PIPO shift register
  - 4-bit input  $in[3:0]$  and 4-bit output  $out[3:0]$



when  $clk = \uparrow$   
 $out[3:0] \leftarrow in[3:0]$

# Johnson Counter

- Recall the SISO shift register
  - By connecting the complementary output of final stage to the input of the SISO shift register, we get the Johnson counter

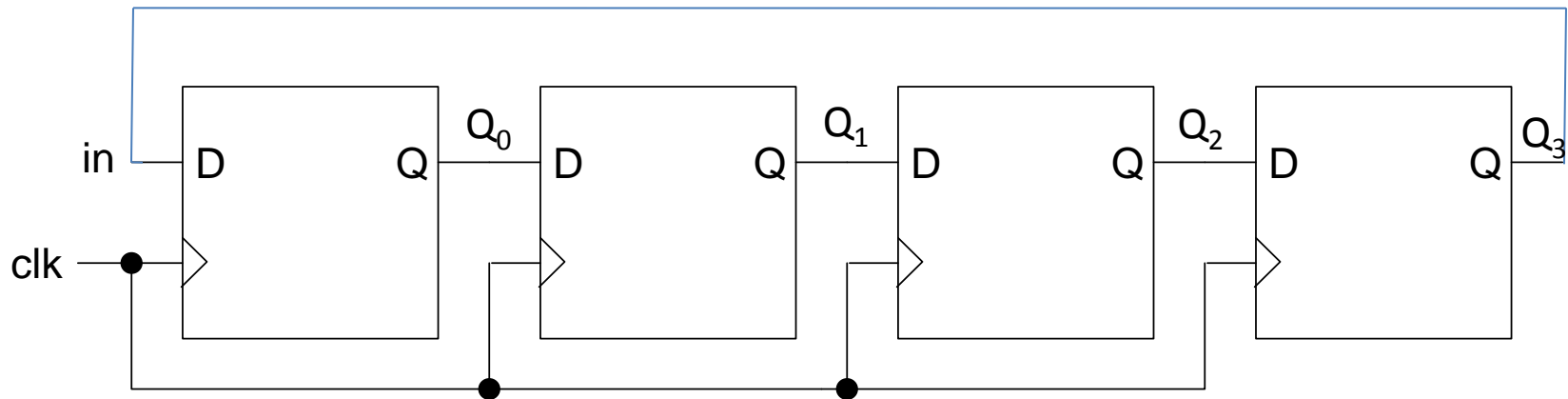


Assume initially  $Q_0 = 0$ ,  $Q_1 = 0$  and  $Q_2 = 0$ , and  $Q_3 = 0$

Determine the values of  $Q_0$ ,  $Q_1$ ,  $Q_2$ , and  $Q_3$  after 8 clock cycles

# Ring Counter

- Again from the SISO shift register,
  - By connecting the output of final stage to the input of the SISO shift register, we get the Ring counter



Assume initially  $Q_0 = 0$ ,  $Q_1 = 0$  and  $Q_2 = 0$ , and  $Q_3 = 0$

At first clock we set  $in = 1$

Determine the values of  $Q_0$ ,  $Q_1$ ,  $Q_2$ , and  $Q_3$  after 8 clock cycles



# Shift Register IC

- Some of the IC's available for shift registers include
  - 74164 – 8-bit SISO shift register
  - 74165 – 8-bit PISO shift register
  - 74194 – 4-bit PIPO shift register
  - 74195 – 4-bit Universal shift register (can be used for SISO, SIPO, and PIPO operations)
  - Refer to datasheet for details