SEE1223: Digital Electronics

6 – Counters and Registers

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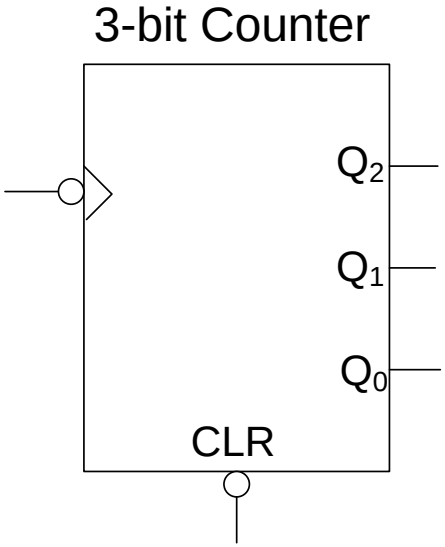
Counter and Registers

- Counters
  - Asynchronous Counters
  - Synchronous Counters
  - Design of Synchronous Counters
  - 74163 devices
- Registers
  - Shift Registers
    - SISO, SIPO, PISO, PIPO
  - Shift Register Counters
    - Johnson and Ring
  - 74164, 74165, 74194, and 74195 devices

Introduction to Counters

- Counters – Circuit that performs the operation of counting at every clock edge



If CLR = 0
    $Q_2Q_1Q_0 = 000$
Else if CLR = 1
    if clk = ↓
        $Q_2Q_1Q_0 = Q_2Q_1Q_0 + 001$
    else
        $Q_2Q_1Q_0 = Q_2Q_1Q_0$

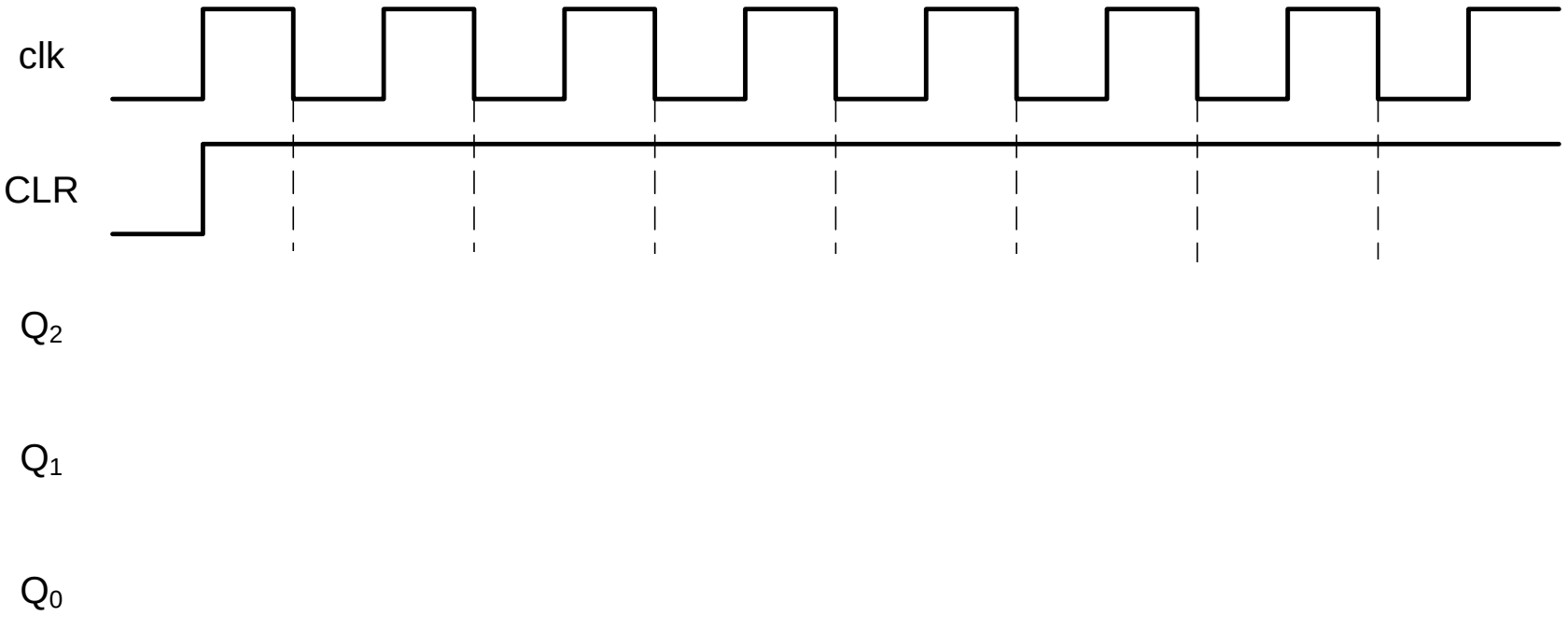
Clear output

Increment by 1 at every Negative edge of clk

Maintain previous value

Introduction to Counters (cont.)

- Draw the output waveforms Q_2, Q_1 and Q_0 for a negative edge triggered 3-bit counter with active low clear

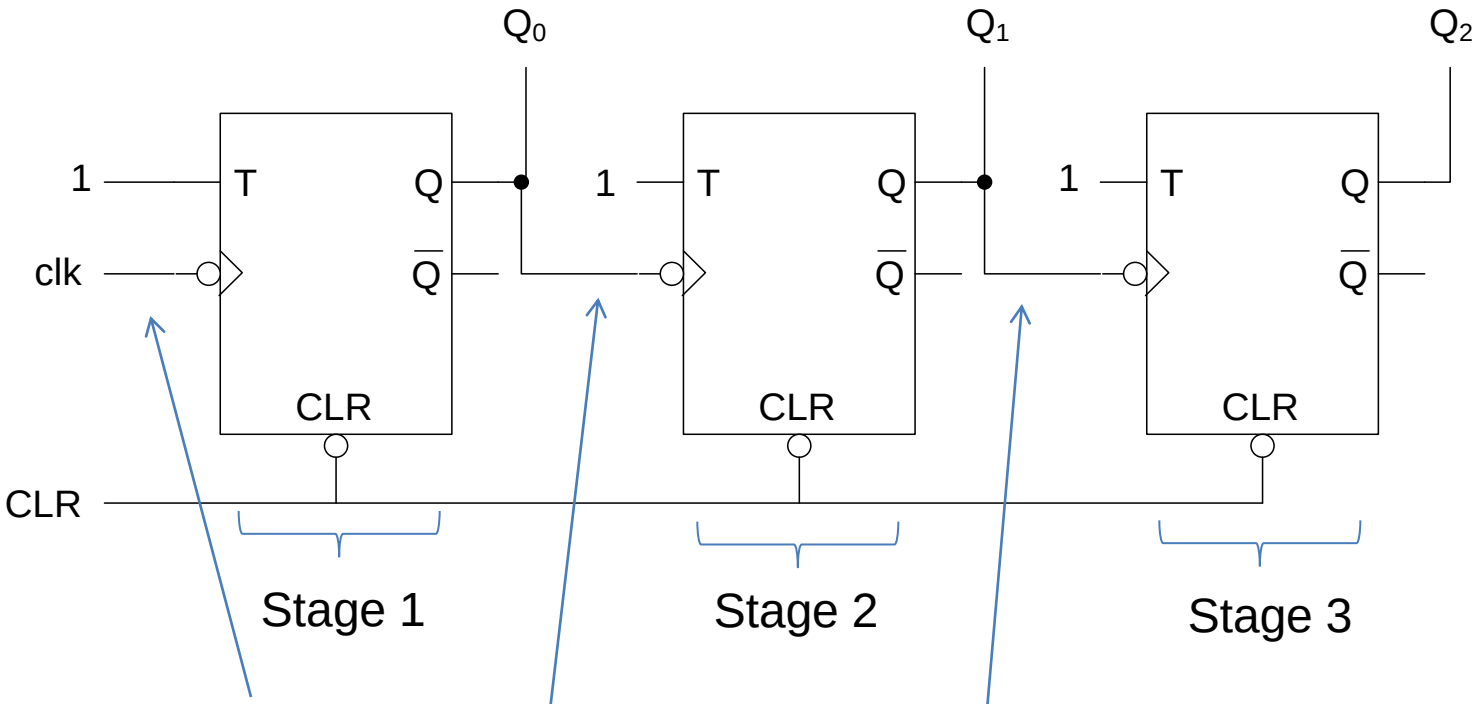


Introduction to Counters (cont.)

- Counter are designed using flip-flops, typically the negative edge triggered
- Counters can be designed as asynchronous or synchronous
- Asynchronous counters – The clock is applied on the first stage. Subsequent stages derive the clock from the previous stage
- Synchronous counters – The clock is applied to all stages using a common clock signal
- Synchronous counters perform better than asynchronous counters, therefore, are widely used in digital systems

Asynchronous Counters

- 3-bit asynchronous counter using T Flip-flops

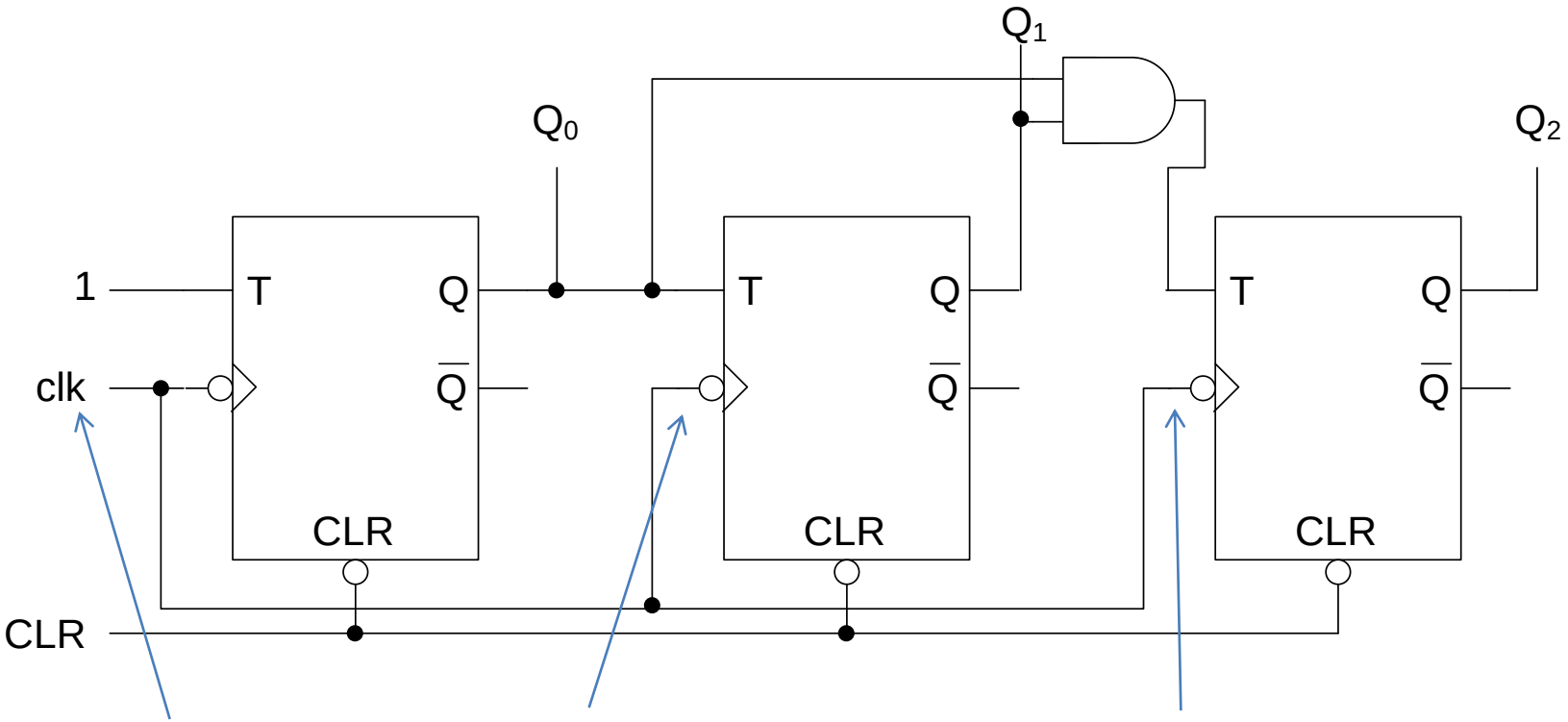


In asynchronous counters, the clk signal is fed to the 1st stage only. Subsequent stages takes the Q from the previous stage for clk

Can you draw the waveform for Q_2, Q_1 and Q_0 for 8 clock cycles?
Can you identify the problem with asynchronous counters?

Synchronous Counters

- 3-bit Synchronous Counter using T Flip-flops



In synchronous counters, a common clk signal is used to clock all flip-flops

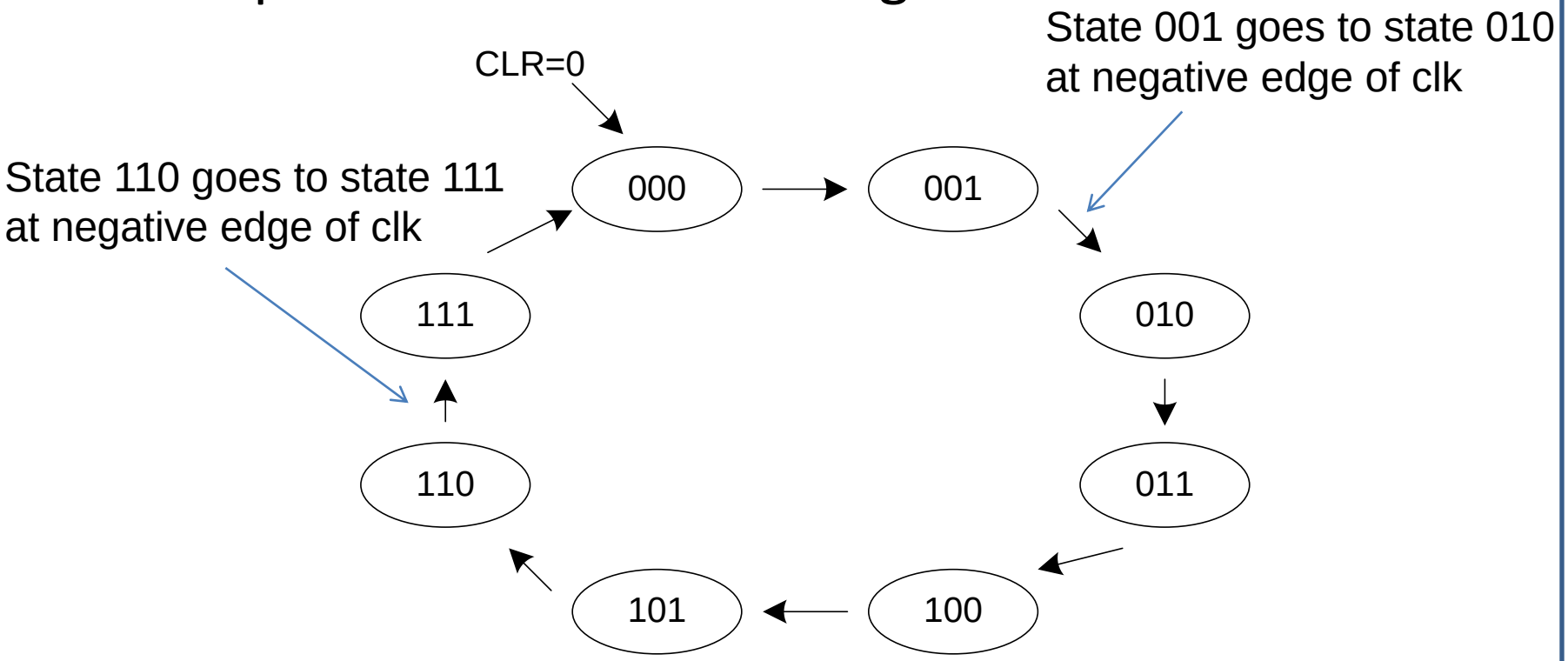
Can you draw the waveform for Q_2, Q_1 and Q_0 for 8 clock cycles?
Why is the synchronous counter superior to asynchronous counters?

Design of Synchronous Counters

- How to design the 3-bit synchronous counter?
  - There is a systematic procedure of designing synchronous counters
    - Step 1: Derive the state transition diagram
    - Step 2: Derive the next state and state transition table
    - Step 3: Using K-Maps, derive the logic expressions
    - Step 4: Implement the circuit

Design of Synchronous Counters

- The design of negative edge triggered 3-bit synchronous counter using T Flip-flops
  - Step 1: Derive the state diagram



Design of Synchronous Counters

- Step 2: Derive the next state and state transition table

3-bit counter, we need 3 flip-flops

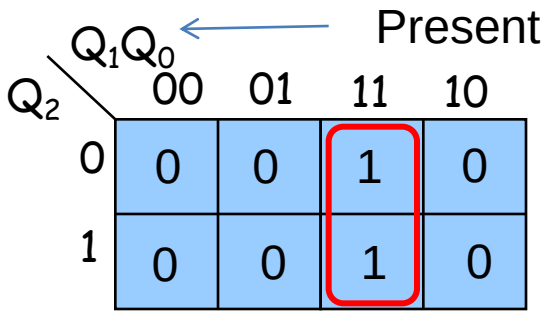
Using T flip-flops

Present State			Next State			Output Transition			Flip-flop Inputs		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0
0	0	0	0	0	1	0→0	0 →0	0 →1	0	0	1
0	0	1	0	1	0	0→0	0 →1	1 →0	0	1	1
0	1	0	0	1	1	0→0	1 →1	0 →1	0	0	1
0	1	1	1	0	0	0→1	1 →0	1 →0	1	1	1
1	0	0	1	0	1	1→1	0 →0	0 →1	0	0	1
1	0	1	1	1	0	1→1	0 →1	1 →0	0	1	1
1	1	0	1	1	1	1→1	1 →1	0 →1	0	0	1
1	1	1	0	0	0	1→0	1 →0	1 →0	1	1	1

Design of Synchronous Counters

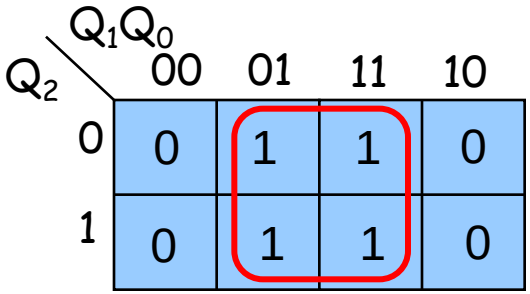
- Step 3: Using K-Maps, derive the logic expressions

K-Map for T_2



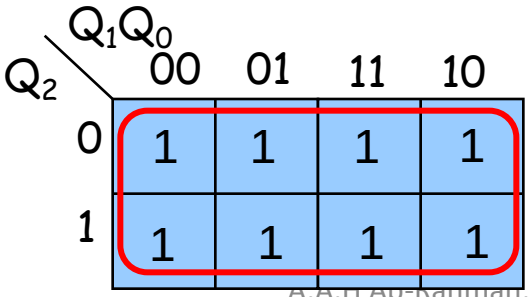
$$T_2 = Q_1 \cdot Q_0$$

K-Map for T_1



$$T_1 = Q_0$$

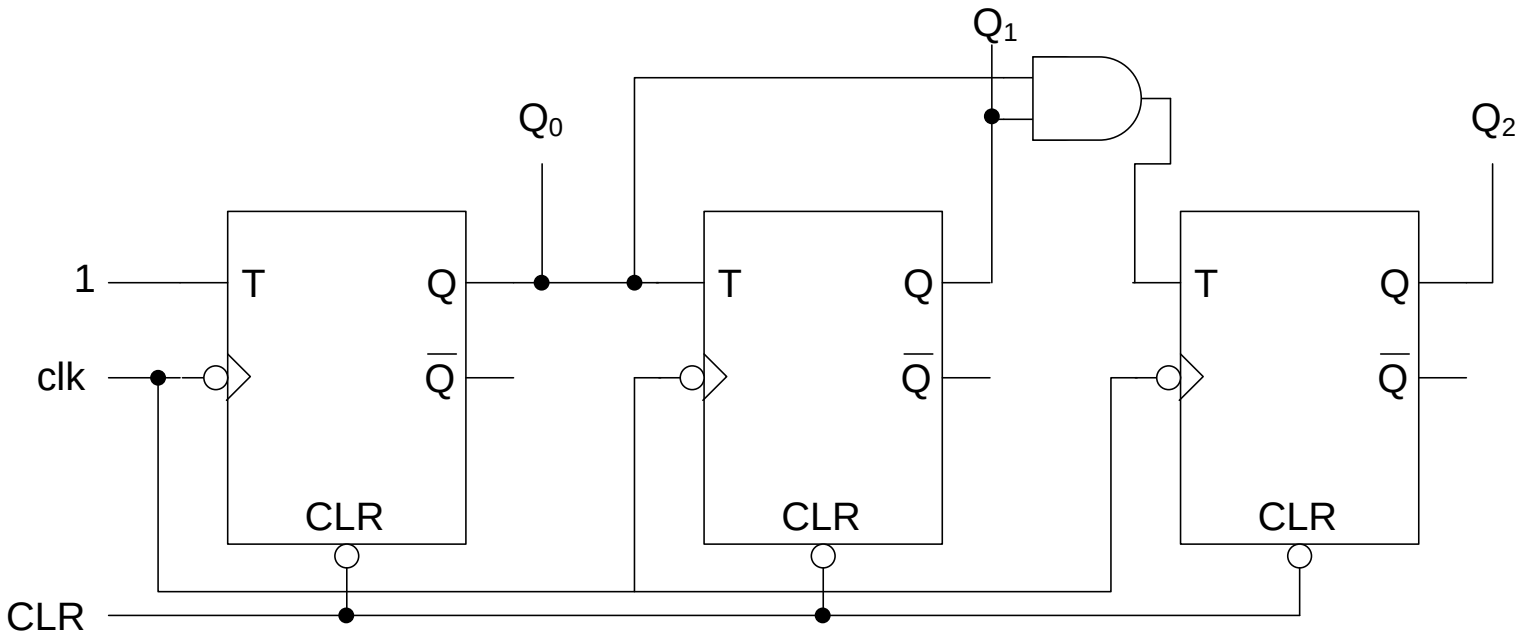
K-Map for T_0



$$T_0 = 1$$

Design of Synchronous Counters

- Step 4: Implement the circuit

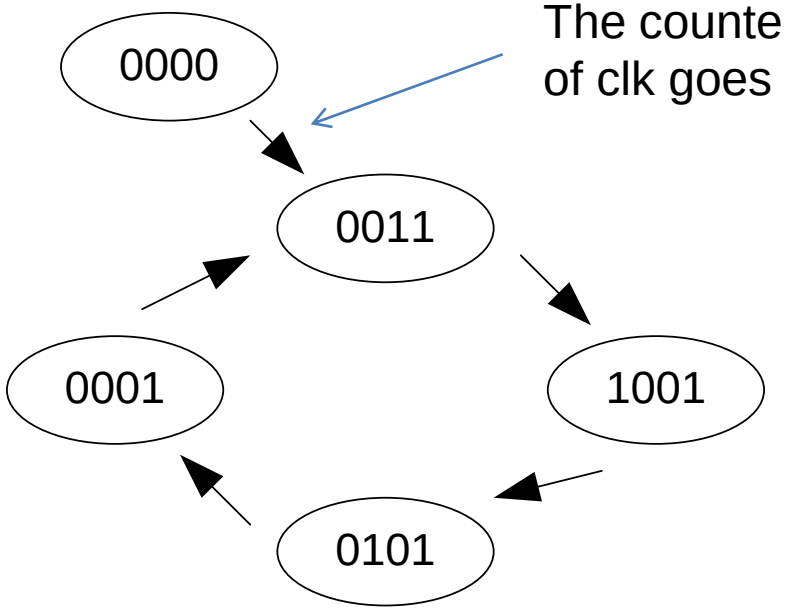


$$T_0 = 1 \qquad T_1 = Q_0 \qquad T_2 = Q_1 \cdot Q_0$$

Which is the same circuit as before

Design of Synchronous Counters

- Implement the following counter using D Flip-flops and basic gates



The counter starts at 0, at next edge of clk goes to 3

The counter counts with the Sequence of 3-9-5-1

How many D Flip-flops do we need?
=> 4

Next step: Derive the next state and state transition table

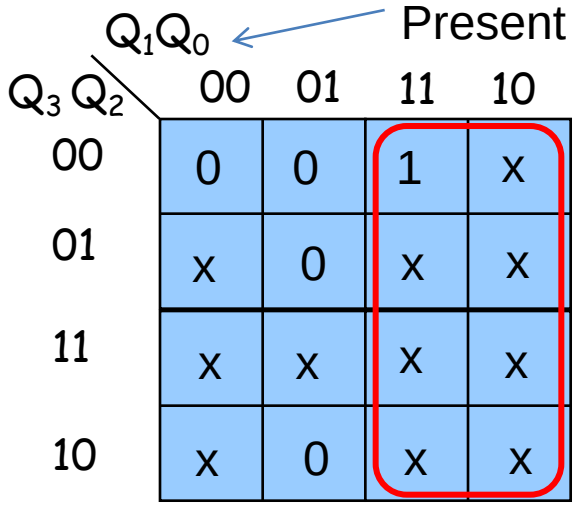
Design of Synchronous Counters

- Next state and state transition table

Present State				Next State				Output Transition				Flip-flop Inputs			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	D_3	D_2	D_1	D_0
0	0	0	0	0	0	1	1	0-0	0-0	0-1	0-1	0	0	1	1
0	0	0	1	0	0	1	1	0-0	0-0	0-1	1-1	0	0	1	1
0	0	1	1	1	0	0	1	0-1	0-0	1-0	1-1	1	0	0	1
0	1	0	1	0	0	0	1	0-0	1-0	0-0	1-1	0	0	0	1
1	0	0	1	0	1	0	1	1-0	0-1	0-0	1-1	0	1	0	1

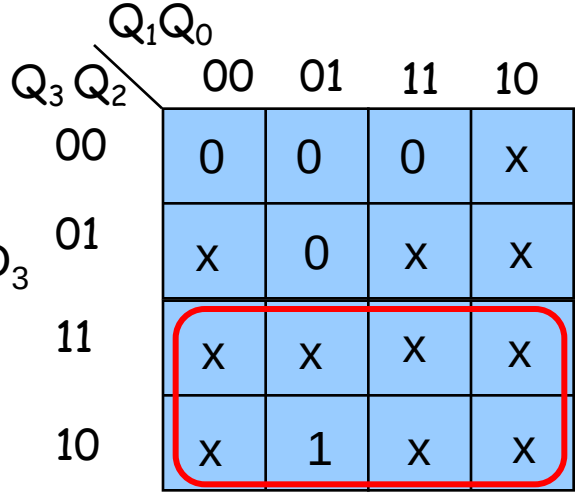
Taking the present state as inputs, use K-Maps to find D_3, D_2, D_1, and D_0
Use don't care conditions when necessary

Design of Synchronous Counters



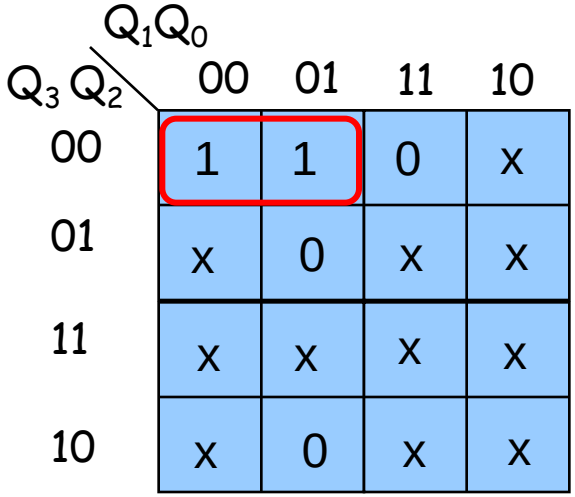
K-Map for D_3

$$D_3 = Q_1$$



K-Map for D_2

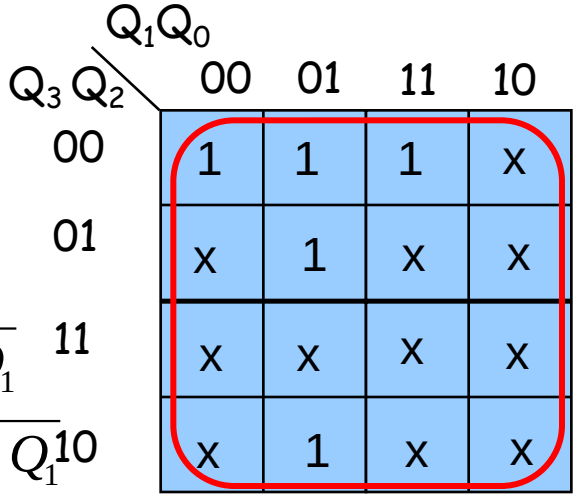
$$D_2 = Q_3$$



K-Map for D_1

$$D_1 = \overline{Q_3} \cdot \overline{Q_2} \cdot \overline{Q_1}$$

$$= \overline{Q_3 + Q_2 + Q_1}$$

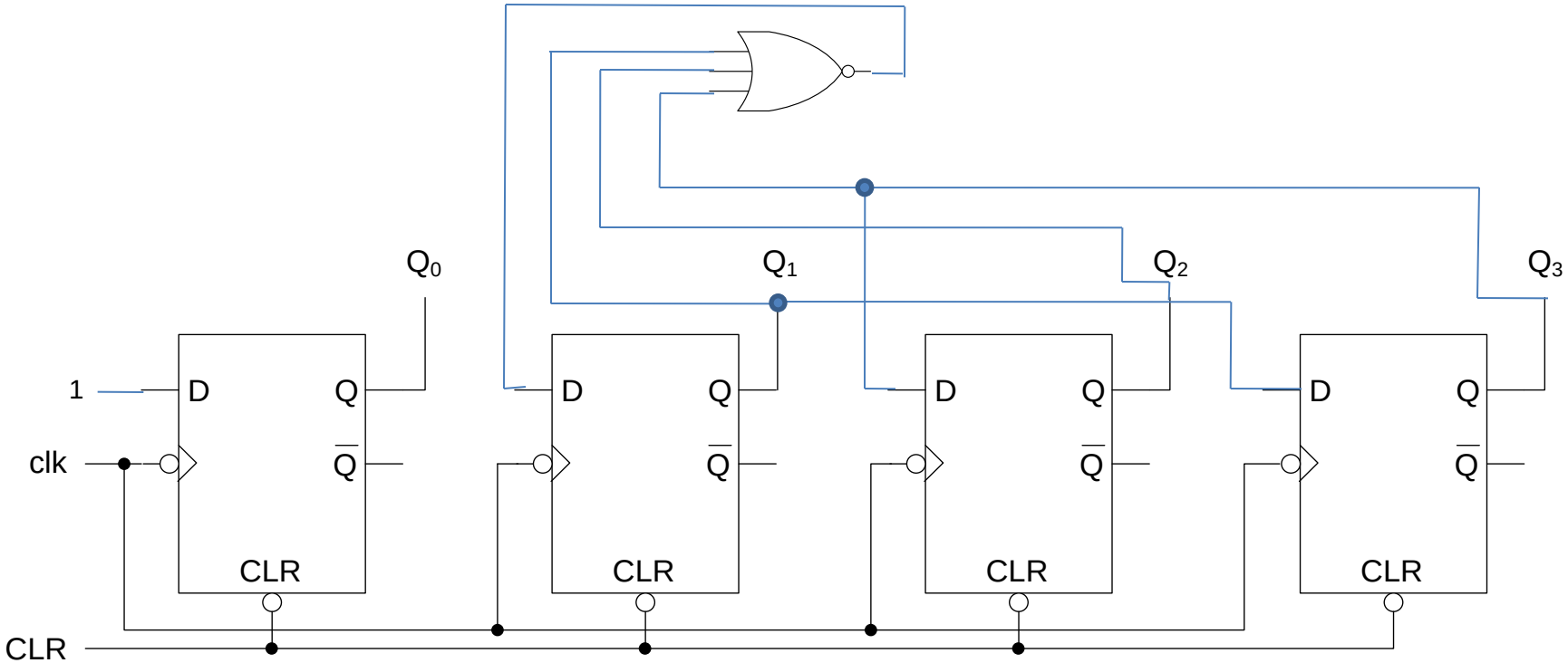


K-Map for D_0

$$D_0 = 1$$

Design of Synchronous Counters

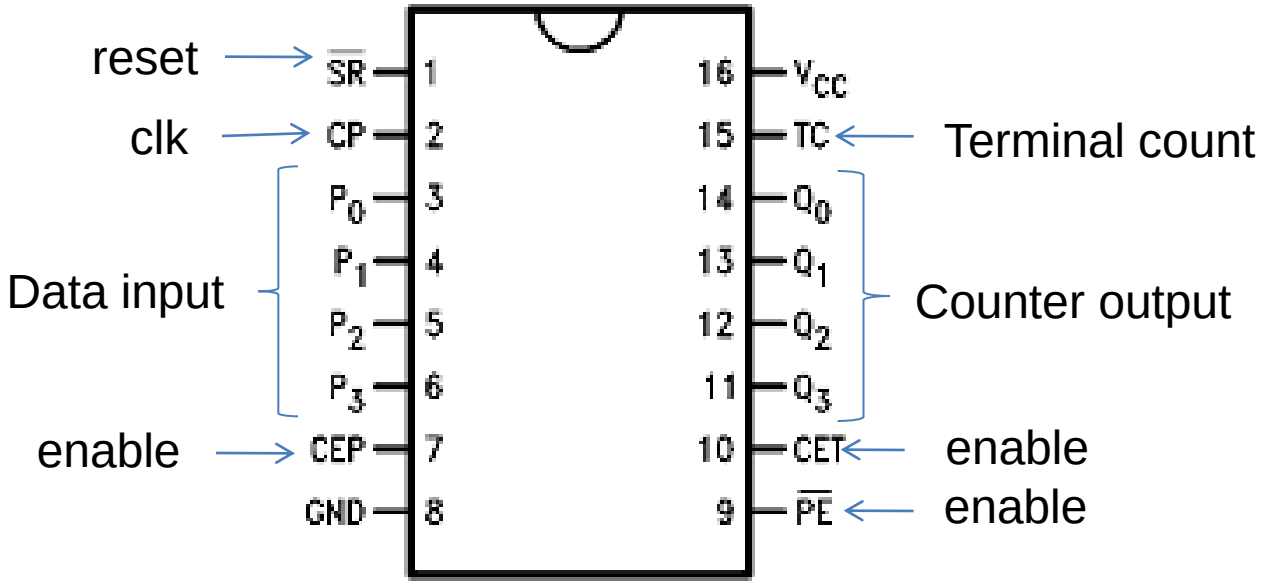
- Final step: Circuit implementation



$$D_0 = 1 \qquad D_1 = \overline{Q_3 + Q_2 + Q_1} \qquad D_2 = Q_3 \qquad D_3 = Q_1$$

Counter IC (cont.)

- The 74163 device: 4-bit Synchronous counter
  - Counts from 0 to 15



Refer to datasheet for details