SEE 3243/4243
Digital System

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Week 5: Arithmetic Circuits Part 1

- Binary Number Representation
  - Sign & Magnitude
  - Ones Complement
  - Twos Complement
- Networks for Binary Addition
  - Half Adder
  - Full Adder
  - Ripple Adder
  - Subtractor

Motivation

- Arithmetic circuits are excellent examples of comb. logic design
- Time vs. Space Trade-offs
  - Doing things fast requires more logic and thus more space
  - Example: carry lookahead logic
- Arithmetic Logic Units
  - Critical component of processor datapath

Unsigned Integers

- Smallest representable value: bit
- Bit groups represent information
- Number of bits determine max. combinations of information
- N bits = 2^N

Number of Bits	Number of values	Machine
4	16	Intel 4004
8	256	8080, 6800
16	65536	PDP11, 8086, 68000
32	~ 4×10^9	IBM 370, 68020, VAX11/780, IEEE single
48	1×10^{14}	Unisys
64	1.8×10^{19}	Cray, IEEE double

Unsigned Integers

- Value for the bit pattern:

$$V_{unsigned} = \sum_{i=0}^{N-1} b_i \times 2^i$$

- Example:

$10110_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$

$= 22_{10}$

- How many numbers can 8-bit represent?
- For N bits, range of values:

0 up to $2^N - 1$

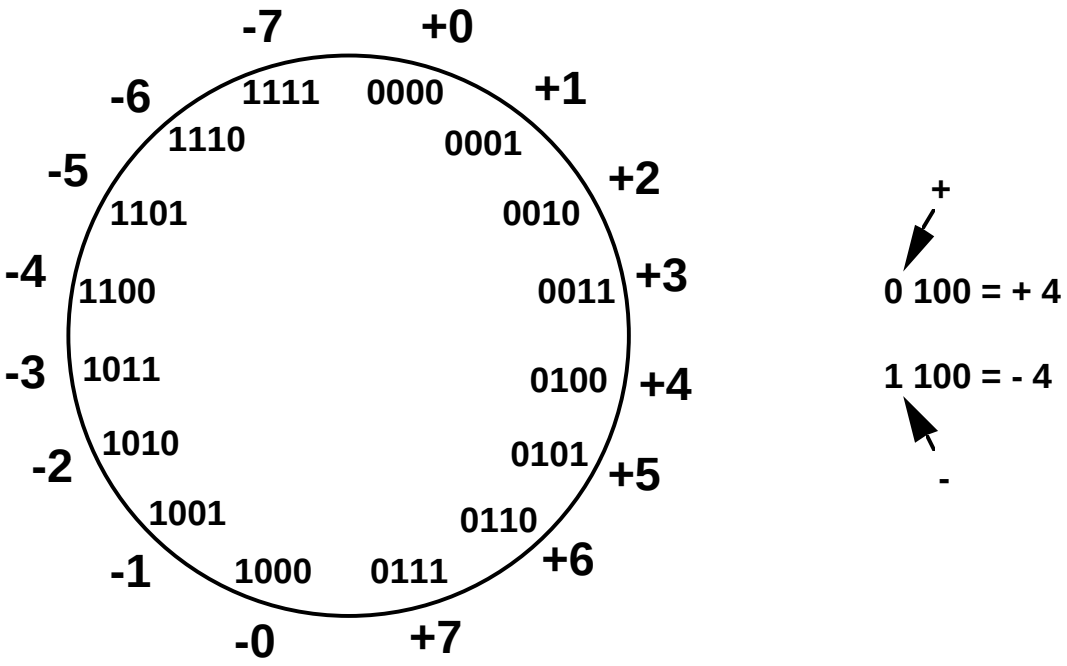
Representation of Negative Numbers

- Representation of positive numbers same in most systems
- Major differences are in how negative numbers are represented
- Three major schemes:
  - sign and magnitude
  - ones complement
  - twos complement
- Assumptions:
  - 4-bit machine word
  - 16 different values can be represented
  - roughly half are positive, half are negative

Sign and Magnitude

- Easiest to understand
- Leftmost bit (MSB) is sign bit
  - 0 means positive
  - 1 means negative
- +18 = 00010010
- -18 = 10010010
- All digit strings with leftmost digit = 0 are positive numbers
- Positive numbers are represented like natural binary numbers
- For a negative number, the magnitude of that number is equal to whatever you get by interpreting all the bits other than the sign bit in the natural way

Sign and Magnitude



- Example for N=4:
  - High order bit is sign: 0 = positive (or zero), 1 = negative
  - Three low order bits is the magnitude: 0 (000) thru 7 (111)
  - Number range for n bits = +/-(2^{n-1}-1)
  - Two representations for 0 (0000 and 1000)

Sign-and-Magnitude Problems

- Easy for humans to understand, but may not be the best for machine operation efficiency
- Cumbersome addition/subtraction
- Must compare magnitudes to determine sign of result
- Need to check both sign and magnitude in arithmetic
- Two representations of zero (+0 and -0)

Ones' Complement Representation

- Ones' complement defined as

$$\overline{N} = (2^n - 1) - N$$

- In ones' complement we get the negation of a number by flipping all the bits
- The name ones' complement comes from the fact that we could also get the negation of a number by subtracting each bit from 1
- Complement of a complement generates original number

Ones' Complement Representation

- Ones' complement of +7
  - Since n=4, $(2^n - 1) = 1111$

$$\overline{N} = (2^n - 1) - N$$

$2^n - 1$	1	1	1	1	
N	0	1	1	1	(+7)
$\overline{N}$	1	0	0	0	(-7)

- Ones' complement of -7

Shortcut method:

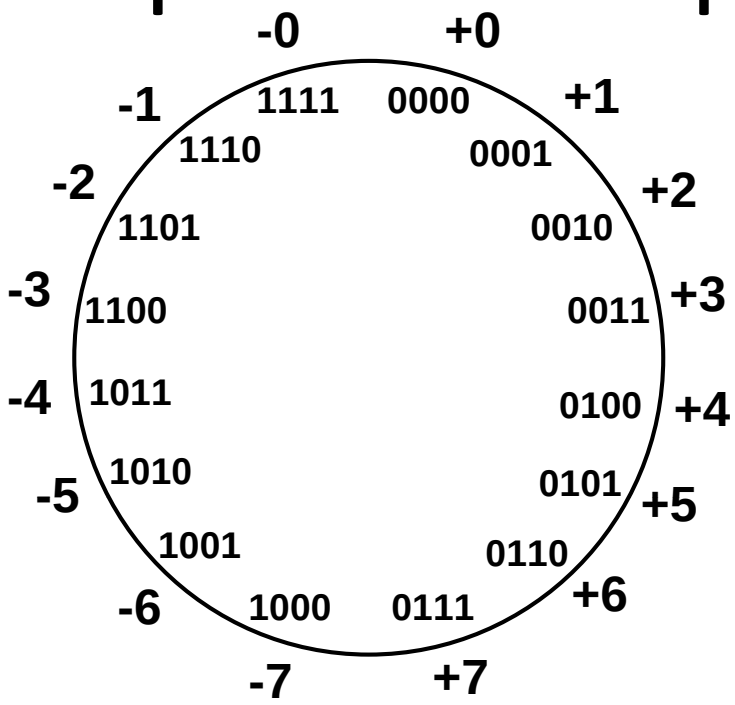
simply compute bitwise complement

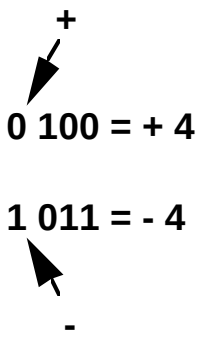
1001 -> 0110

$2^n - 1$	1	1	1	1	
N	1	0	0	0	(-7)
$\overline{N}$	0	1	1	1	(+7)

Ones' Complement Representation

$\overline{N} = (2^n - 1) - N$





- Some complexities in addition
- Subtraction implemented by addition & 1's complement
- Still two representations of 0! This causes some problems

Two's Complement

- Two's complement defined as

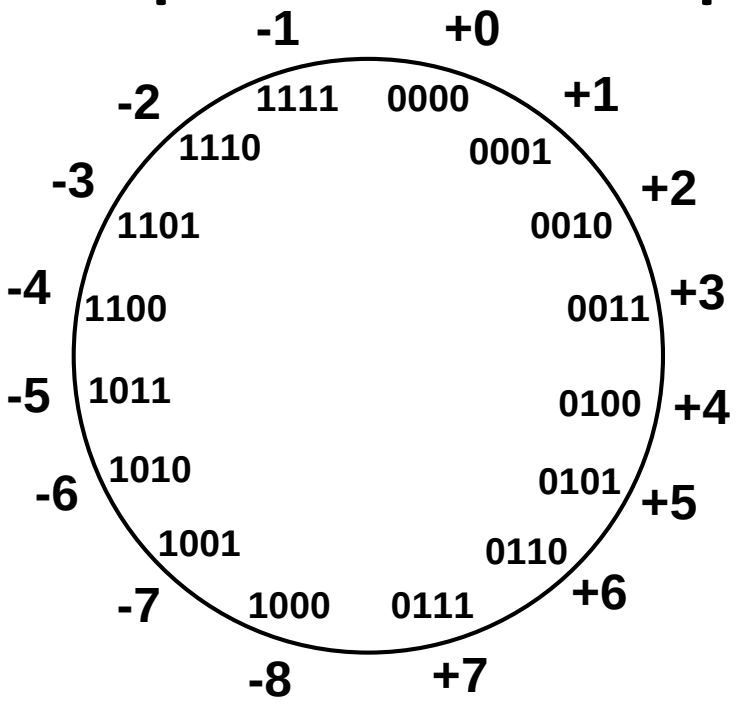
$$N^* = 2^n - N \text{ for } N \neq 0$$

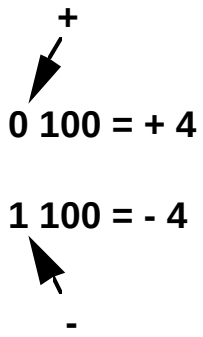
$$0 \text{ for } N = 0$$

- Exception is so result will always have n bits
- Two's complement is just a 1 added to 1's complement
- Complement of a complement generates original number

Twos Complement Representation

like 1's comp except shifted one position clockwise





- Only one representation for 0
- One more negative number than positive number

Two's Complement Representation

$N^* = 2^n - N$

- Two's complement of +7

2^n	1 0000	
N	0111	(+7)
N*	1001	(-7)

- Two's complement of -7

2^n	1 0000	
N	1001	(-7)
N*	0111	(+7)

Shortcut method:
Twos complement = bitwise complement + 1

0111 -> 1000 + 1 -> 1001 (representation of -7)

1001 -> 0110 + 1 -> 0111 (representation of 7)

Finding 2's Complement

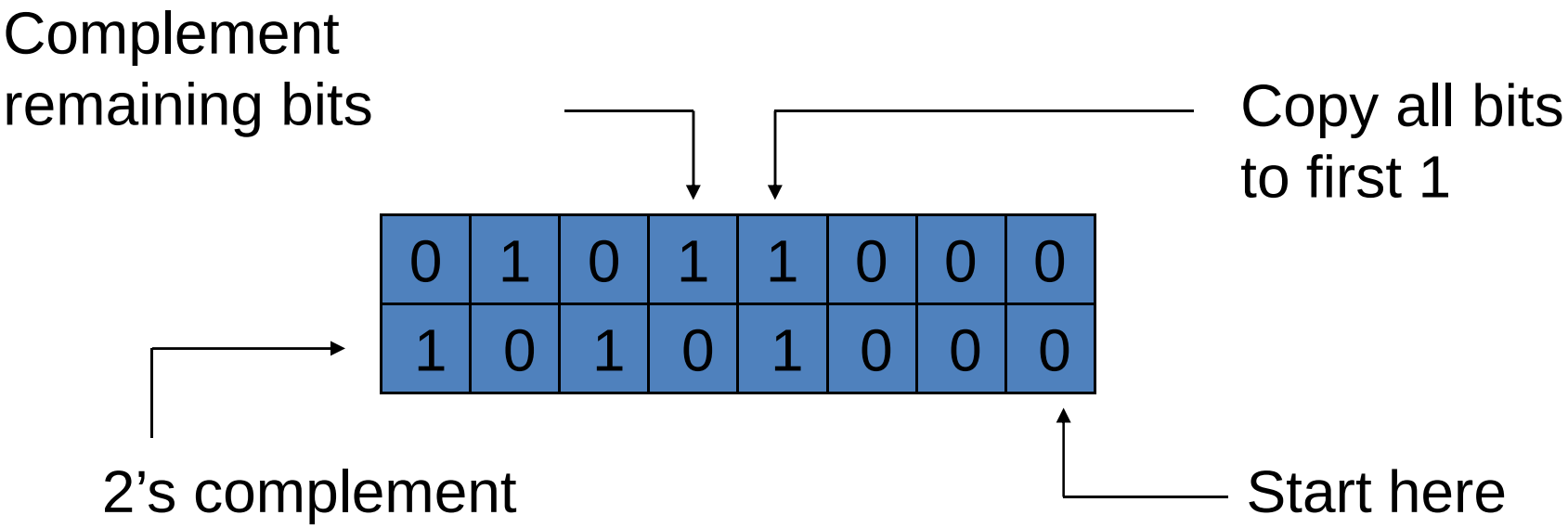


Table 2-6 Decimal and 4-bit numbers.

Decimal	*Two's Complement*	*Ones' Complement*	*Signed Magnitude*
–8	1000	—	—
–7	1001	1000	1111
–6	1010	1001	1110
–5	1011	1010	1101
–4	1100	1011	1100
–3	1101	1100	1011
–2	1110	1101	1010
–1	1111	1110	1001
0	0000	1111 or 0000	1000 or 0000
1	0001	0001	0001
2	0010	0010	0010
3	0011	0011	0011
4	0100	0100	0100
5	0101	0101	0101
6	0110	0110	0110
7	0111	0111	0111

Range of Numbers

- 4-bit 2s complement
  - +7 = 0111 = 2^3-1
  - -8 = 1000 = -2^3
- 8 bit 2s complement
  - +127 = 01111111 = 2^7 -1
  - -128 = 10000000 = -2^7
- 16 bit 2s complement
  - +32767 = 011111111 11111111 = 2^{15} - 1
  - -32768 = 100000000 00000000 = -2^{15}
- N bit 2s complement
  - 011111111..11111111 = $2^{N-1} – 1$ (largest positive)
  - 100000000..00000000 = -2^{N-1} (largest negative)

Conversion Between Lengths, e.g. 8 → 16

- Positive number: add leading zeros
  - +18 = 00010010
  - +18 = 00000000 00010010
- Negative numbers: add leading ones
  - -18 = 11101110
  - -18 = 11111111 11101110
- i.e. pack with msb (sign bit)

called "sign extension"

Addition and Subtraction

- a – b = ?
- Normal binary addition
- Monitor sign bit of result for overflow

- Take negation of b and add to a
  - i.e. a – b = a + (– b)
- So we only need addition and complement circuits

Addition and Subtraction : Ones Complement

4	0100	-4	1011
+ 3	0011	+ (-3)	1100
7	0111	-7	10111
		End around carry	→ 1
			1000

4	0100	-4	1011
- 3	1100	+ 3	0011
1	10000	-1	1110
End around carry	→ 1		
	0001		

Addition and Subtraction : Twos Comp

4	0100	-4	1100
+ 3	0011	+ (-3)	1101
7	0111	-7	11001

If carry-in to sign = carry-out then ignore carry

4	0100	-4	1100
- 3	1101	+ 3	0011
1	10001	-1	1111

If carry-in to sign = carry-out then ignore carry

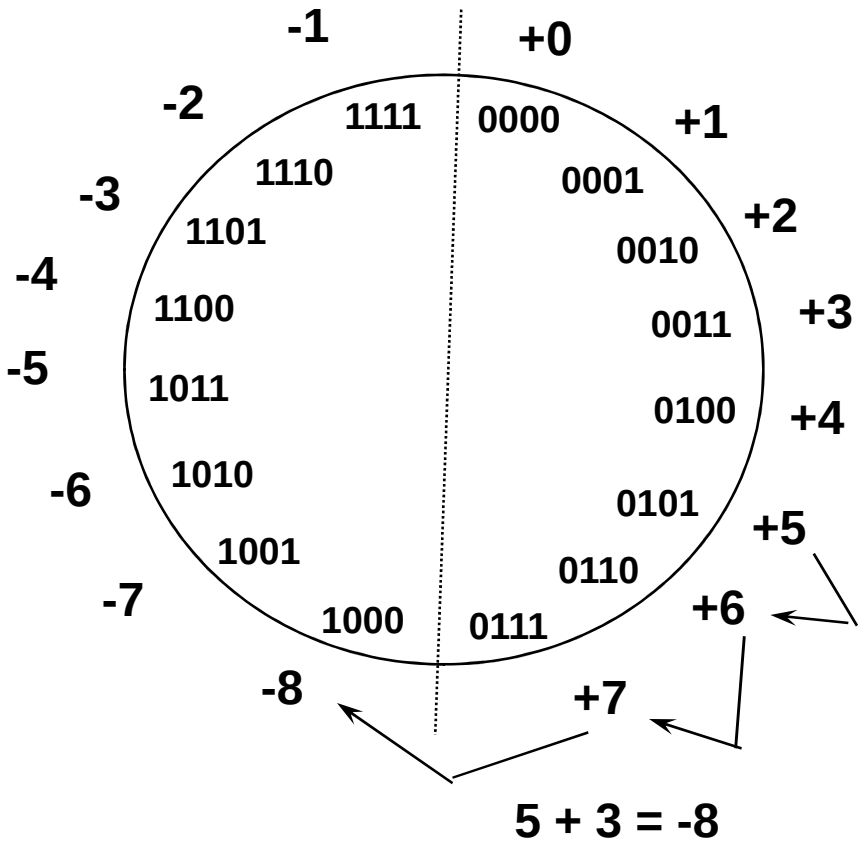
- Simpler addition scheme makes twos complement the most common choice for integer number systems within digital systems

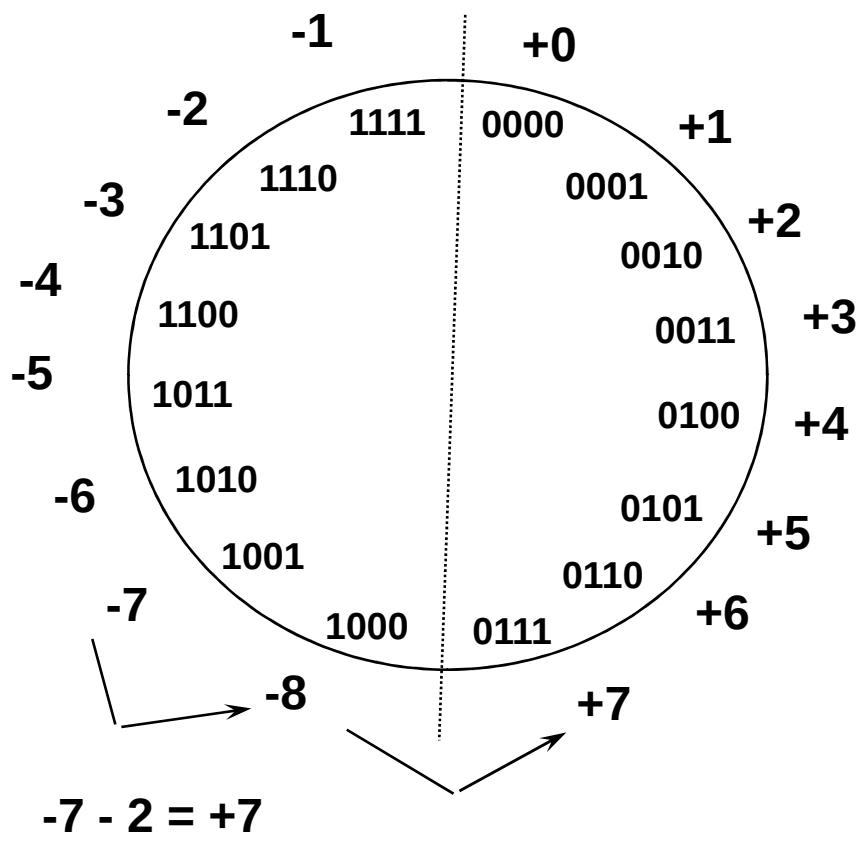
Addition and Subtraction : Twos Comp

- Why can the carry-out be ignored?
- Add 2's complement of N to M
  - This is M - N = M + N*
- If $M \geq N$, will generate carry
  - $M + N^* = M + (2^n - N) = M - N + 2^n$
  - Discard carry: just like subtracting 2^n
  - Result is positive M - N
- If $M < N$, no carry

Overflow Conditions

- Add two positive numbers to get a negative number or two negative numbers to get a positive number





Twos Complement Overflow

	Expected	0 1 1 1	Actual
	+5	0 1 0 1	
+	+3	0 0 1 1	
	+8	1 0 0 0	-8

Overflow

	Expected	1 0 0 0	Actual
	-7	1 0 0 1	
+	-2	1 1 1 0	
	-9	0 1 1 1	+7

Overflow

	Expected	0 0 0 0	Actual
	+5	0 1 0 1	
+	+2	0 0 1 0	
	+7	0 1 1 1	+7

No Overflow

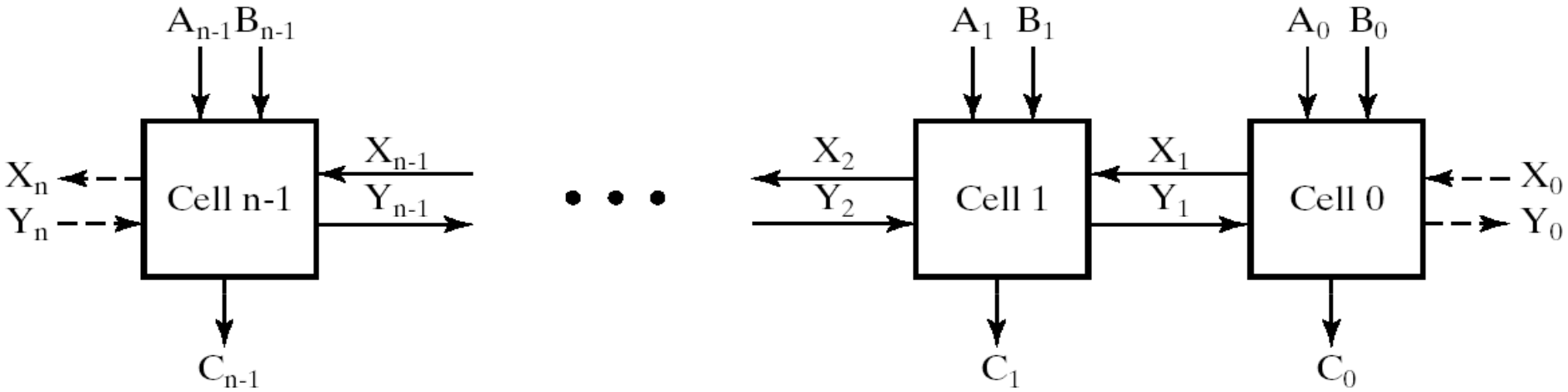
	Expected	1 1 1 1	Actual
	-3	1 1 0 1	
+	-5	1 0 1 1	
	-8	1 0 0 0	+8

No Overflow

Overflow when carry in to sign does not equal carry out

Iterative Circuit

- Like a hierarchy, except functional blocks per bit



- Adders are a great example of this type of design
- Design 1-bit circuit, then expand
- Look at
  - Half adder – 2-bit adder, no carry in
    - Inputs are bits to be added
    - Outputs: result and possible carry
  - Full adder – includes carry in, really a 3-bit adder

Half Adder

- Simplest adder block is “half adder”
  - Not very useful by itself

X	Y	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

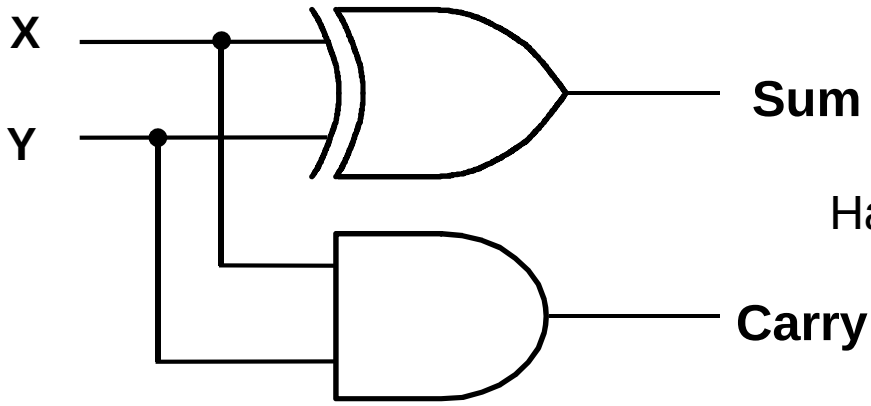
Y \ X	0	1
0	0	0
1	0	1

Carry = A B

Y \ X	0	1
0	0	1
1	1	0

Sum = A’ B + A B’

= A ⊕ B



Half-adder Schematic

Full Adders

- Basic building block is full adder
- Many full-adders are combined to add more than 1 bits
- Truth table:

x	y	c_{in}	c_{out}	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full Adder

C_{in} \ XY	00	01	11	10
0	0	1	0	1
1	1	0	1	0

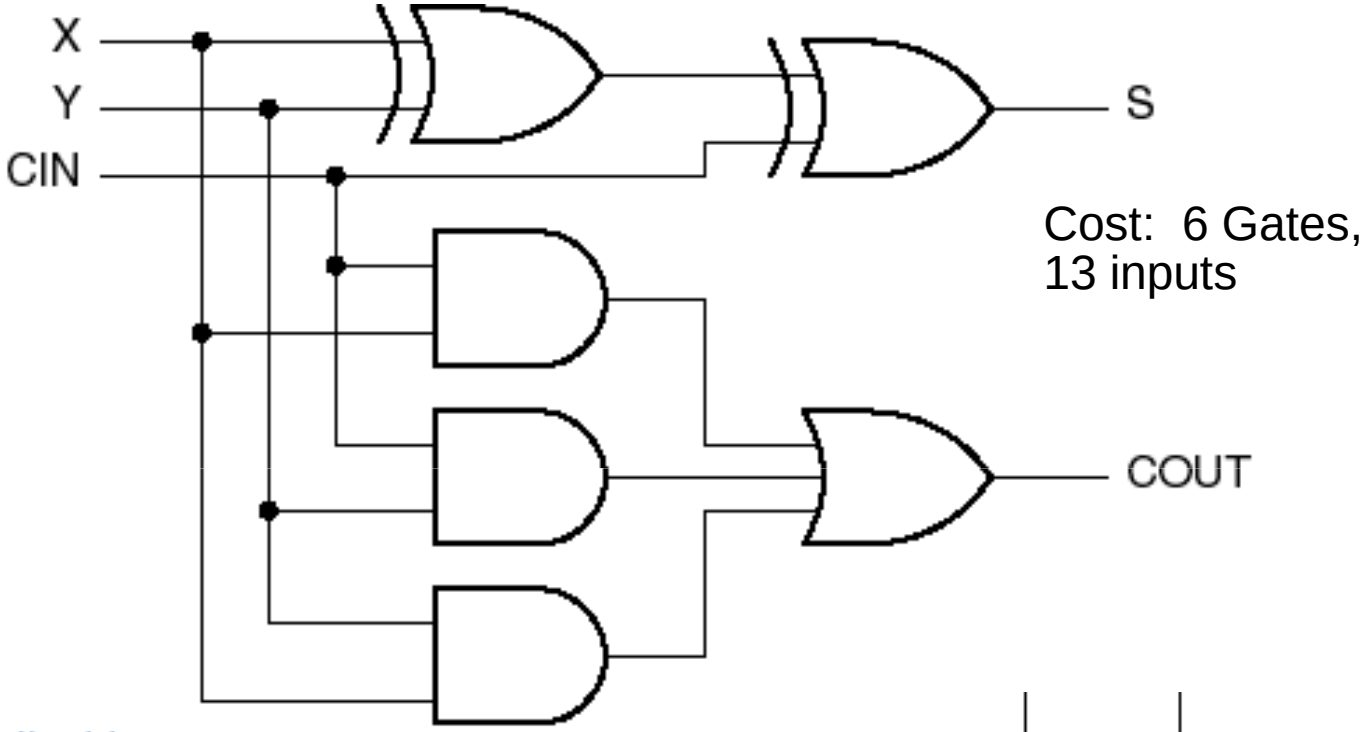
$$S = X \oplus Y \oplus C_{in}$$

C_{in} \ XY	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$C_{out} = X\,Y + X\,C_{in} + Y\,C_{in}$$
$$= X\,Y + (X + Y)\,C_{in}$$

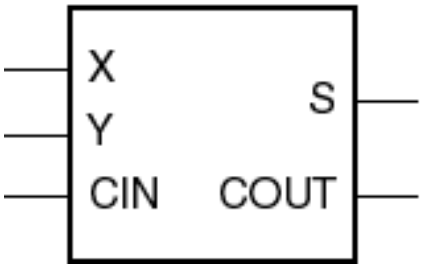
- In a multi-stage adder:
  - Variable i indicates stage number.
  - C_{in} is carry to i-th stage, also known as C_i
  - C_{out} is carry to next stage, also known as C_{i+1}

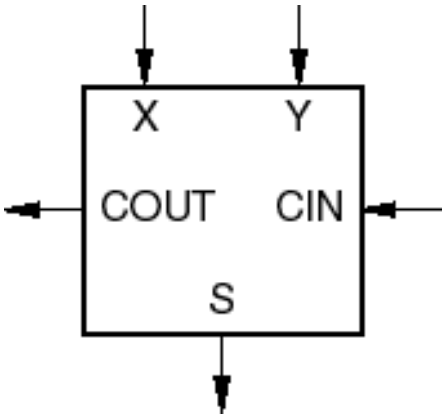
Full-adder circuit: Straightforward Approach



Cost: 6 Gates,
13 inputs

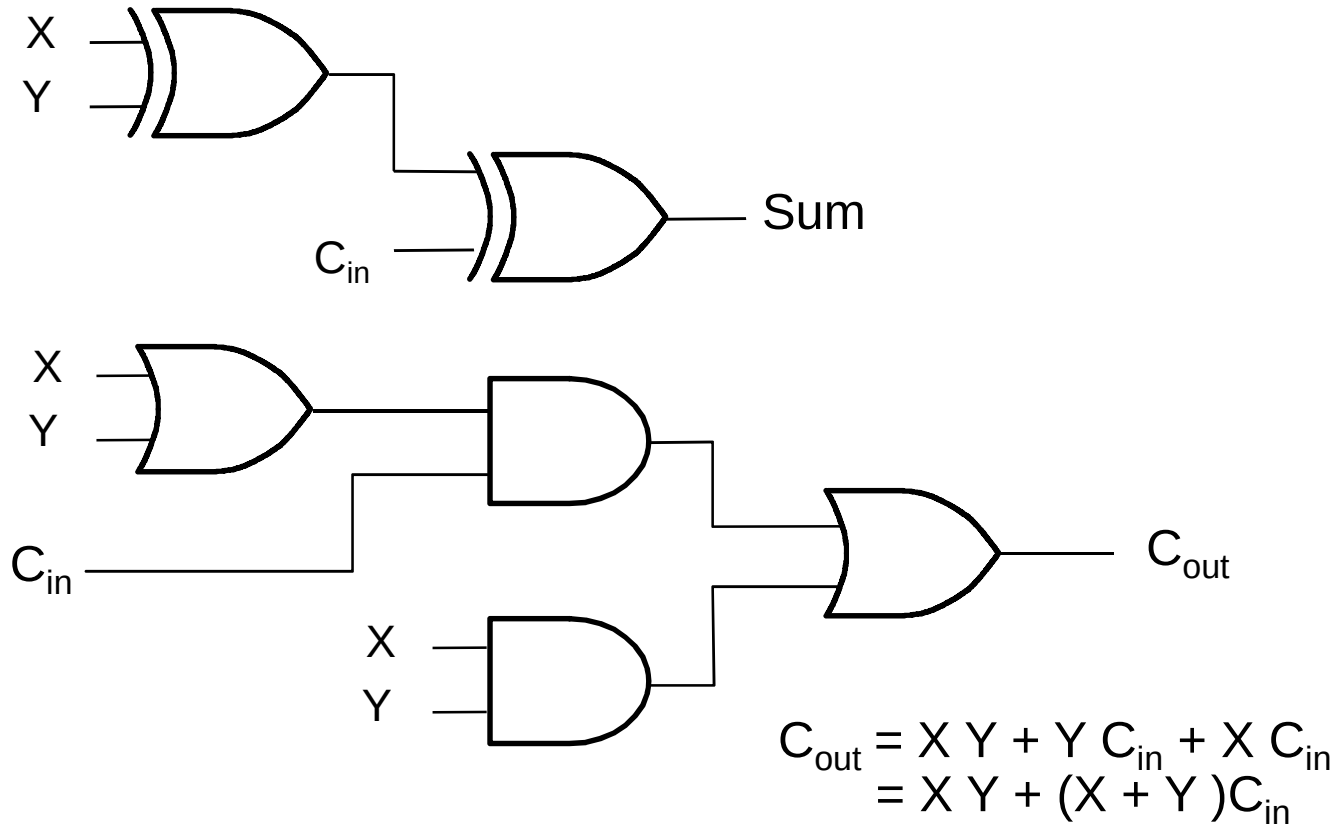
full adder





Full Adder: Alternative Implementation

- Cost: 6 Gates, max. 2 inputs per gate, 3 levels of logic
- Advantage: All gates of 2-input type, easier to do VLSI layout



$$C_{out} = X\,Y + Y\,C_{in} + X\,C_{in}$$
$$= X\,Y + (X + Y)\,C_{in}$$

Implementation with Two Half Adders (and an OR)

Cost: 5 Gates, 3 levels of logic

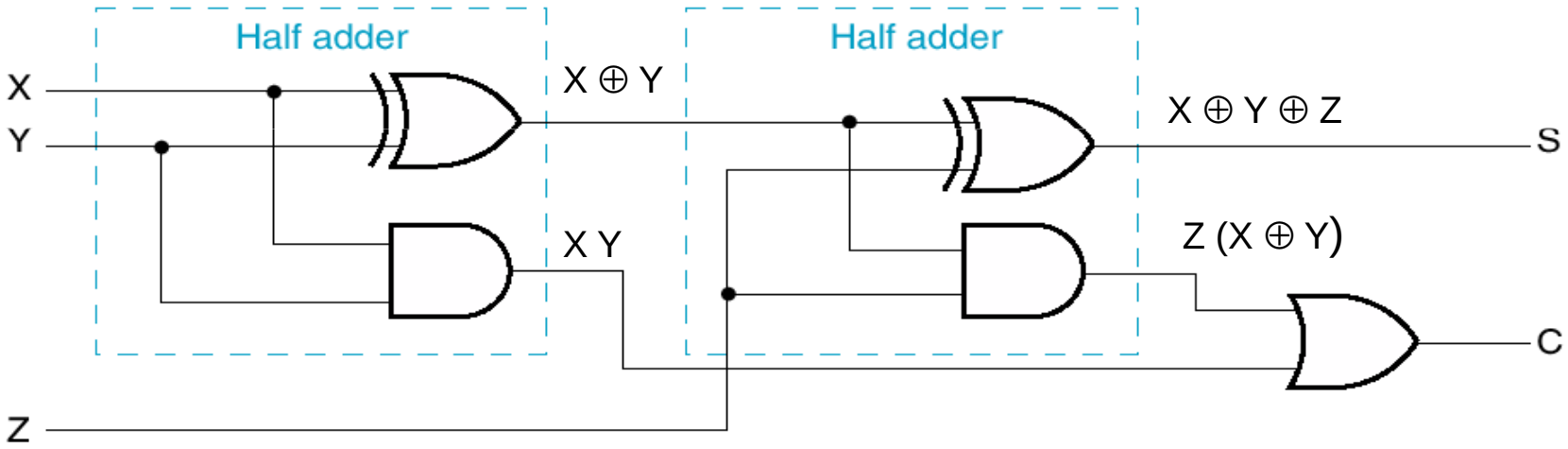
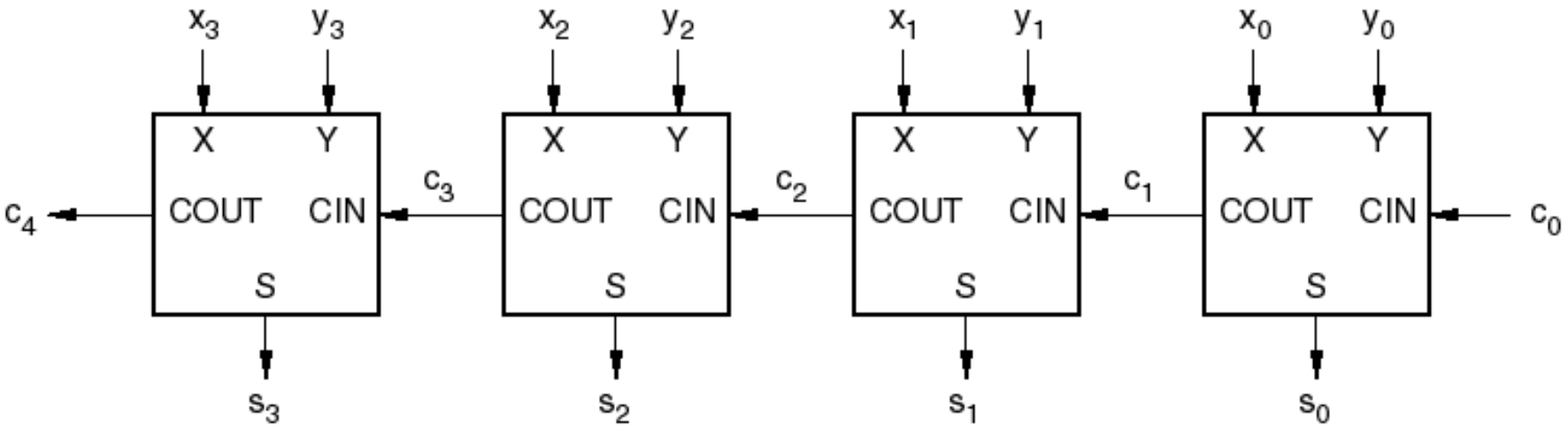


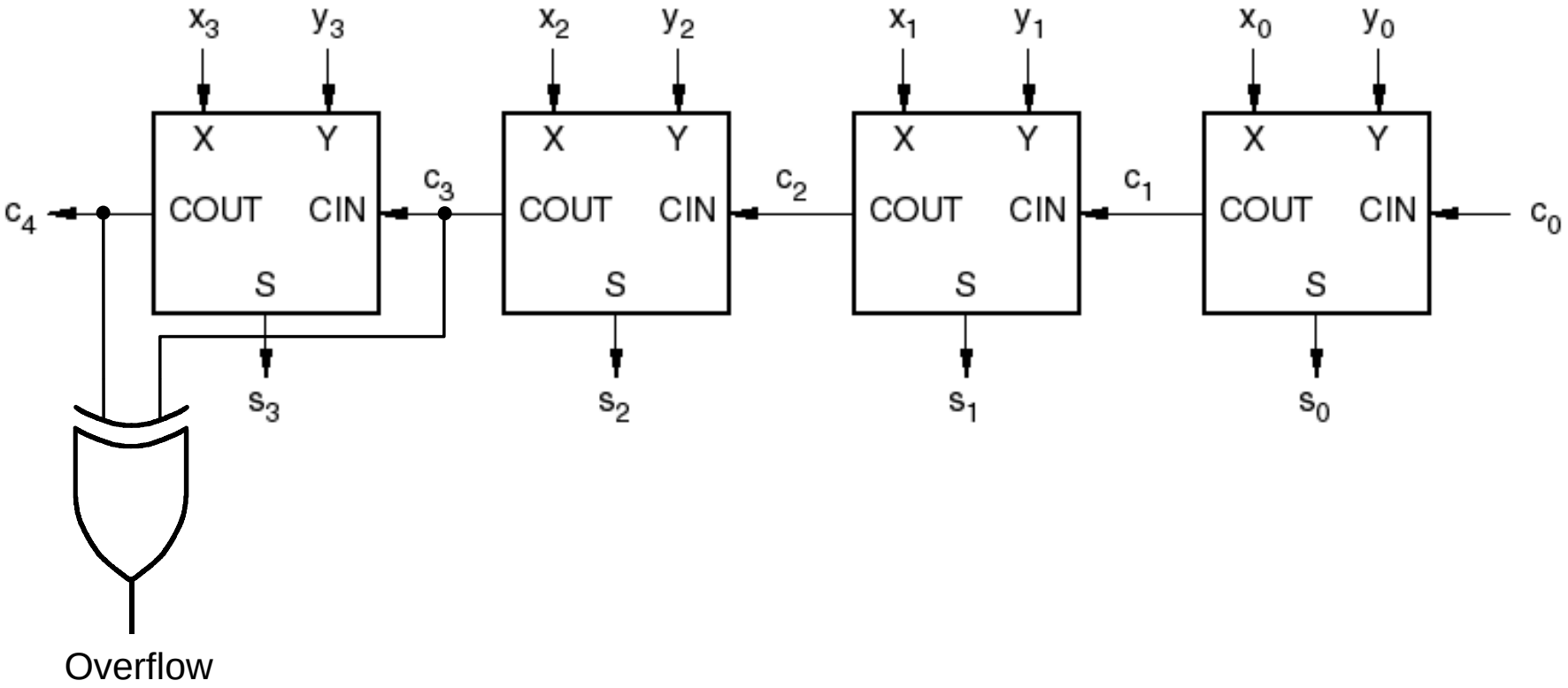
Fig. 3-27 Logic Diagram of Full Adder

Ripple-Carry Adder



- Straightforward – connect full adders
- Carry-out to carry-in chain
  - C_0 in case this is part of larger chain, maybe just set to zero
- Speed limited by carry chain
- Faster adders eliminate or limit carry chain
  - 2-level AND-OR logic ==> 2^n product terms
  - 3 or 4 levels of logic, carry lookahead

Overflow Detection



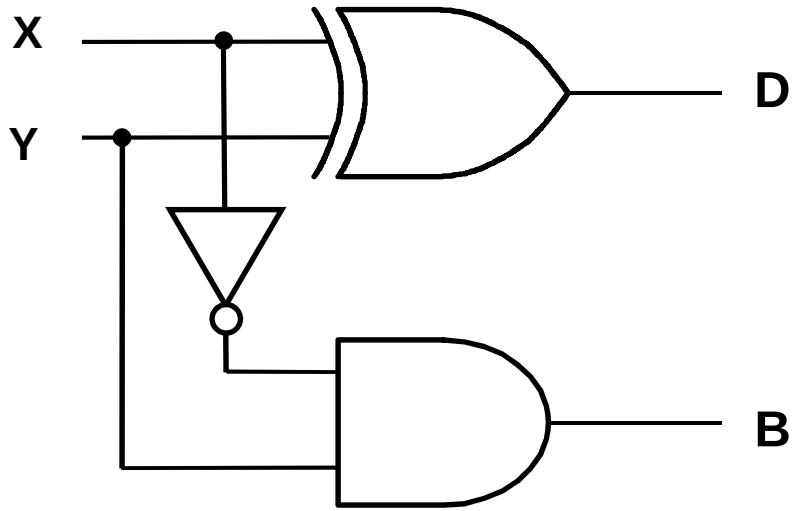
- If Overflow = 1, then overflow condition occurs. The output should not be used, i.e. the output is wrong.
- Condition is that either C_{n-1} or C_n is high, but not both (n = #stages)

Half Subtractor Circuit

X	Y	B	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

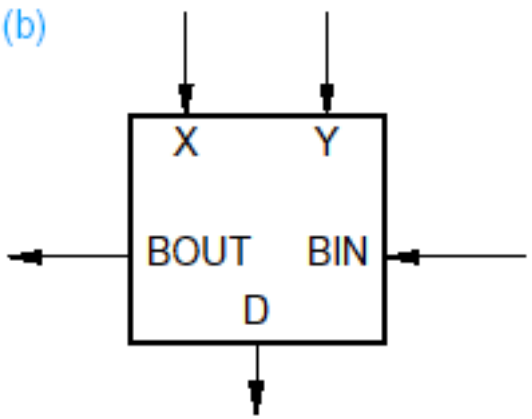
Difference
$D = X'Y + XY' = X \oplus Y$

Borrow
$B = X'Y$



Full Subtractor Circuit

X	Y	B_{in}	B_{out}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

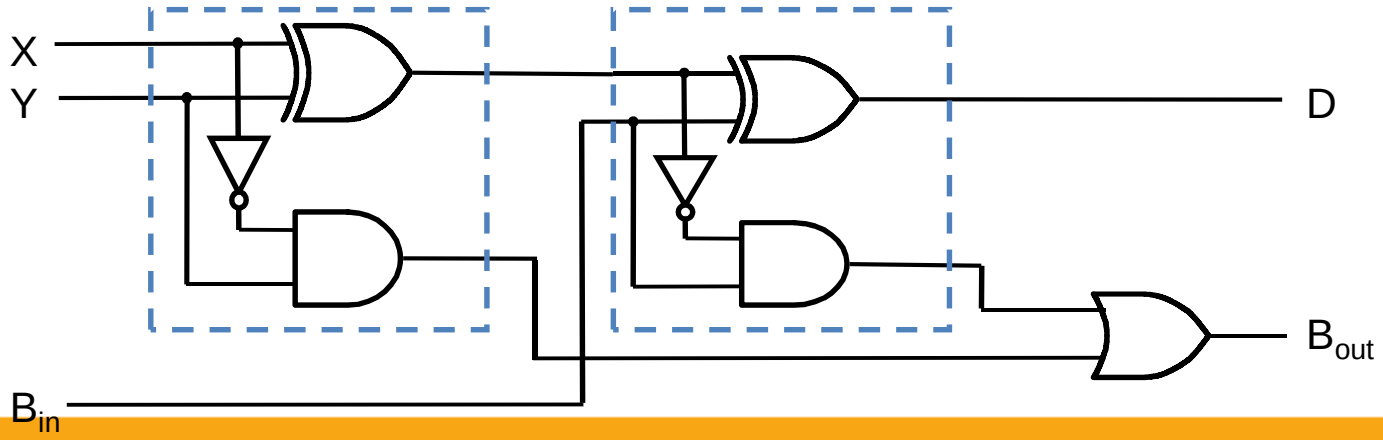


Difference

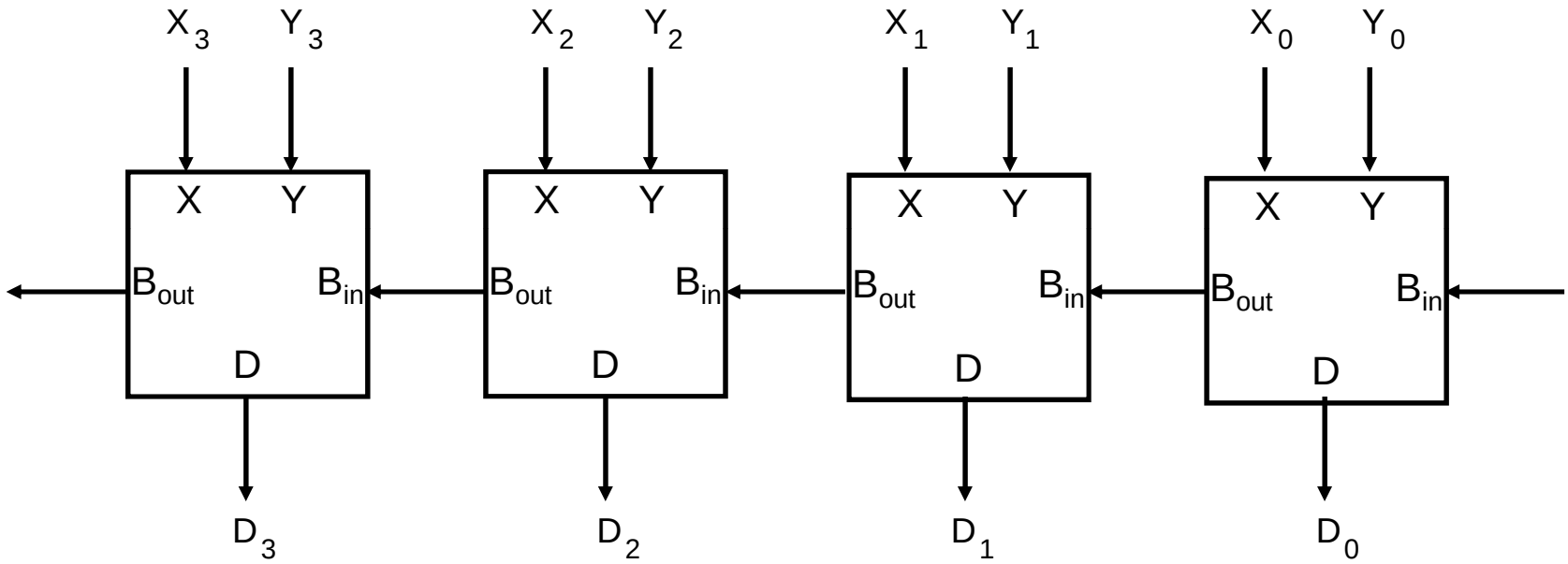
$D = X \oplus Y \oplus B_{in}$

Borrow out

$B_{out} = X'Y + X'B_{in} + YB_{in}$

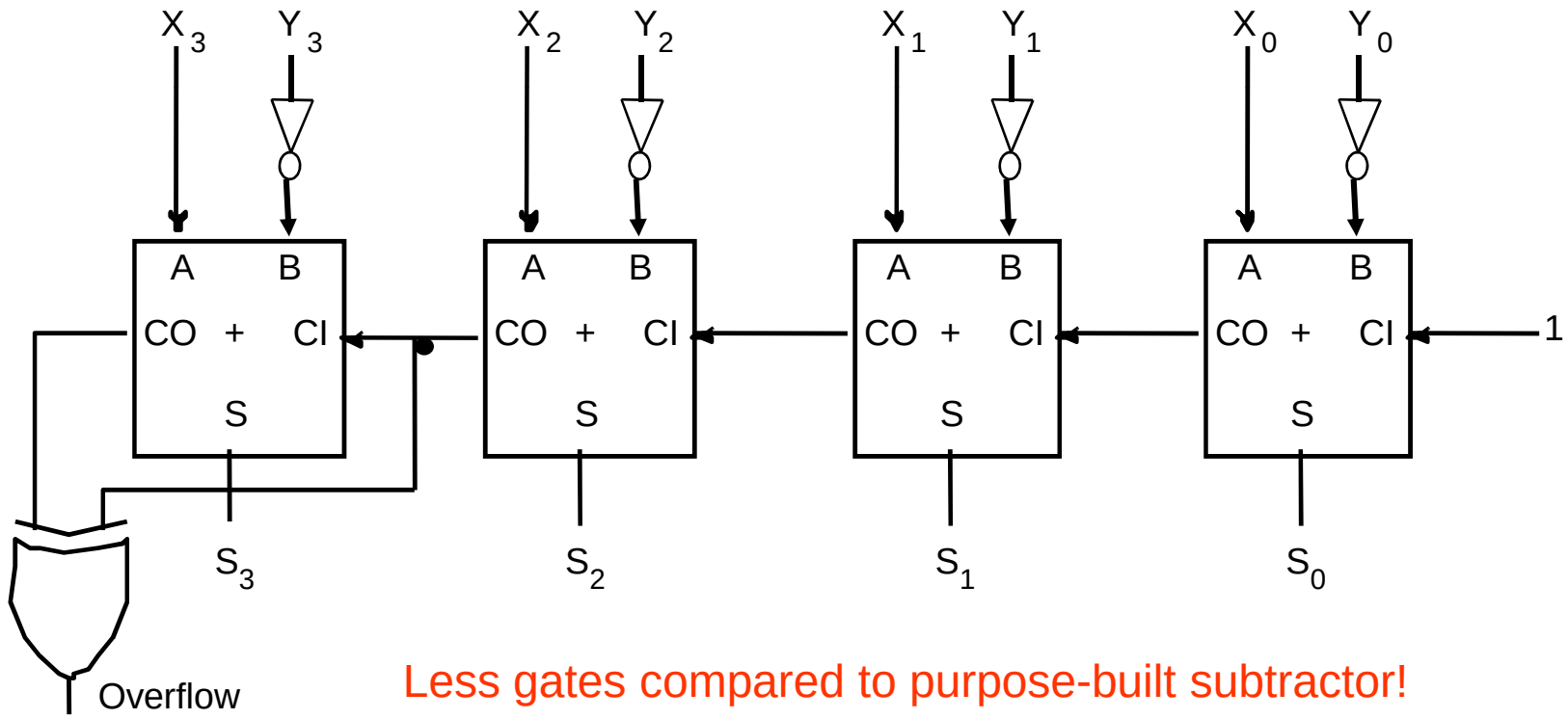


Multi-Stage Full Subtractor



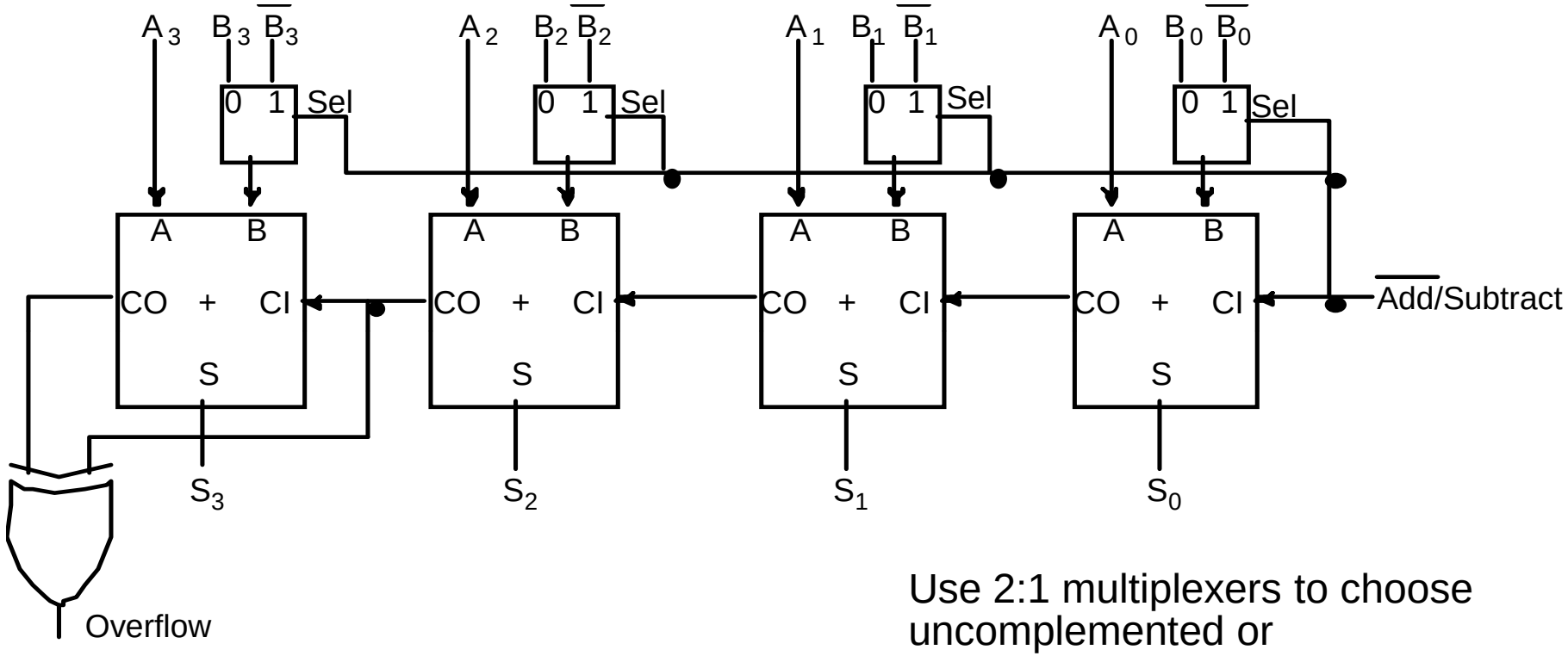
Subtraction Using Adders

- Subtraction is the same as addition of the two's complement.
- The two's complement is the bit-by-bit complement plus 1.
- Therefore, X – Y = X + Y' + 1 .
  - Complement Y inputs to adder, set C_I to 1.



Less gates compared to purpose-built subtractor!

Adder/Subtractor



Use 2:1 multiplexers to choose uncomplemented or complemented inputs

Remember, A - B = A + (-B) = A + $\overline{B}$ + 1
So when Add/Sub = 0, S = A + B
When Add/Sub = 1, S = A + $\overline{B}$ + 1 = A - B

Alternative Design

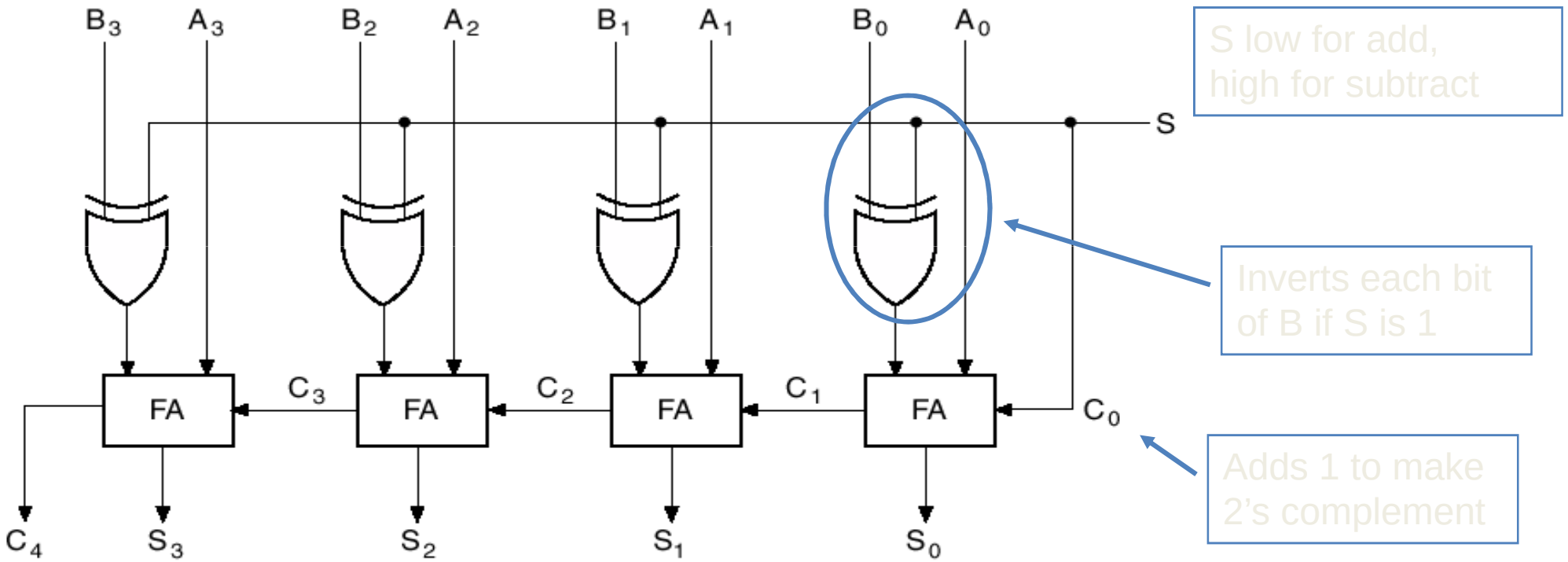


Fig. 3-31 Adder-Subtractor Circuit

- Output is 2's complement if B > A