Digital Electronics (SKEE1223)

Digital Integrated Circuits

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Logic Families

- TTL
- CMOS
- BiCMOS

Logic Family Overview

- TTL
  - Transistor-Transistor Logic
  - Uses bipolar junction transistors (BJT)
- CMOS
  - Complimentary Metal Oxide Semiconductor
  - Uses Metal Oxide Semiconductor Field Effect Transistors (MOSFET)
- BiCMOS
  - Combines TTL & CMOS

TTL vs CMOS

TTL	CMOS
• Inexpensive • Draw a lot of power • Must be supplied with +5 volts • Each gate usually uses 10mW	• Dissipates low power. Consumption depends on supply voltage, switching frequency, output load and input rise time. • A typical gate uses only 10nW.

More on CMOS

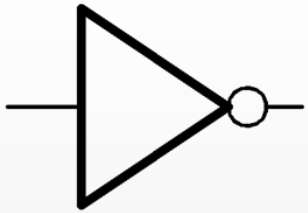
- CMOS components are more expensive but at the system level, CMOS is less expensive. This is because CMOS chips are smaller and require less power regulation.
- CMOS circuits use almost no power at rest. However, current draw increases with switching frequency.
- CMOS component more likely to be damaged due electrostatic discharge.


Logic levels
Switching speed
Component Parameters
Power dissipation
Fan-out
Noise immunity

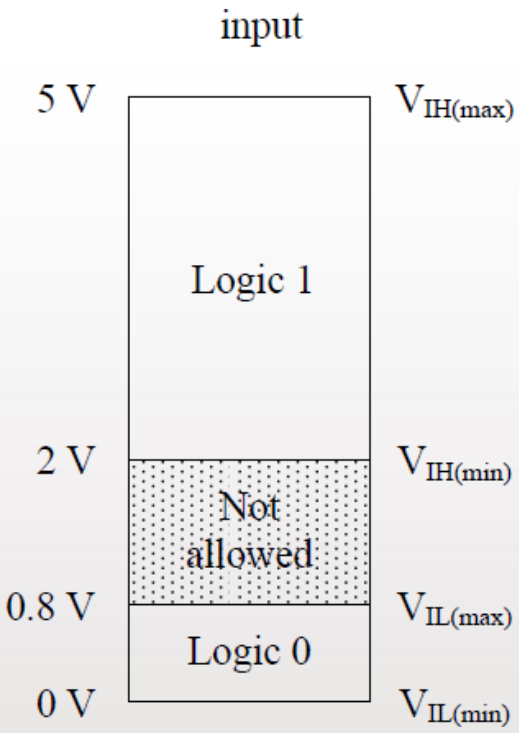
Logic Levels

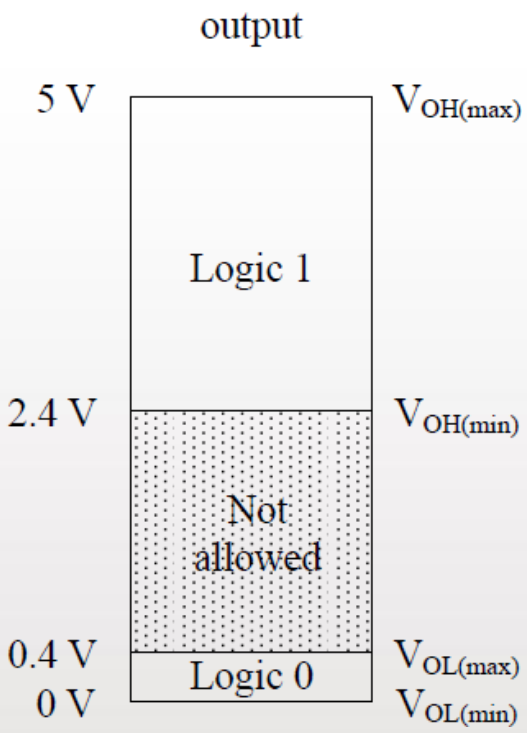
	TTL	CMOS
Supply voltage	5V (V_{CC})	3 to 15V (V_{DD})
Logic 0	0 to 0.8V	0 to 1/3 V_{DD}
Logic 1	2V to 5V	2/3 V_{DD} to V_{DD}

TTL Logic Levels

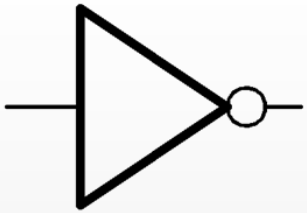


V_{IL}	LOW input Voltage
V_{IH}	HIGH input Voltage
V_{OL}	LOW output Voltage
V_{OH}	HIGH output Voltage





CMOS Logic Levels



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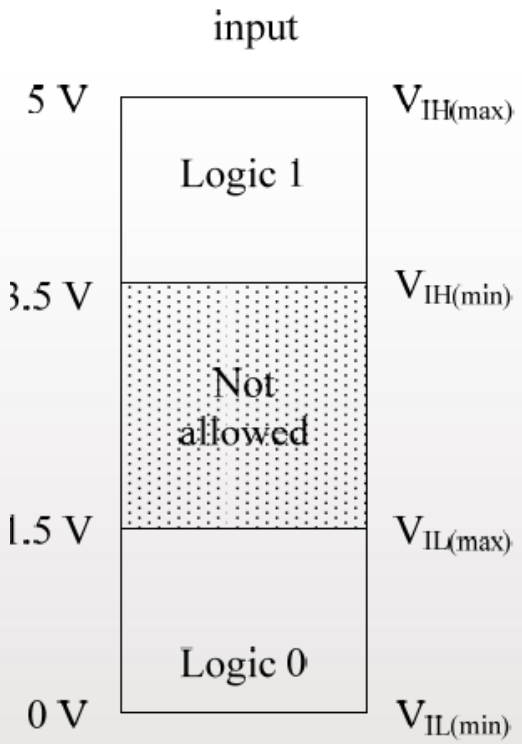
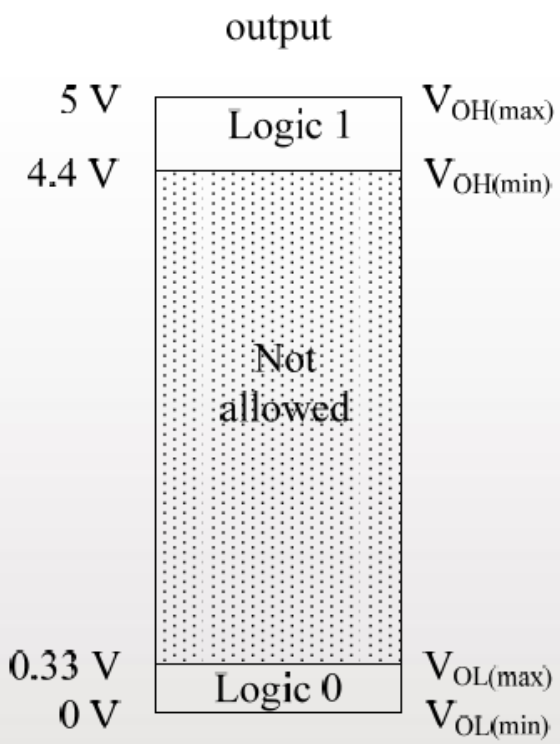
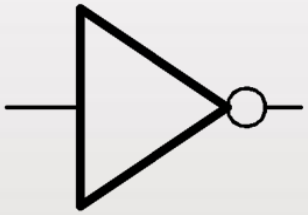
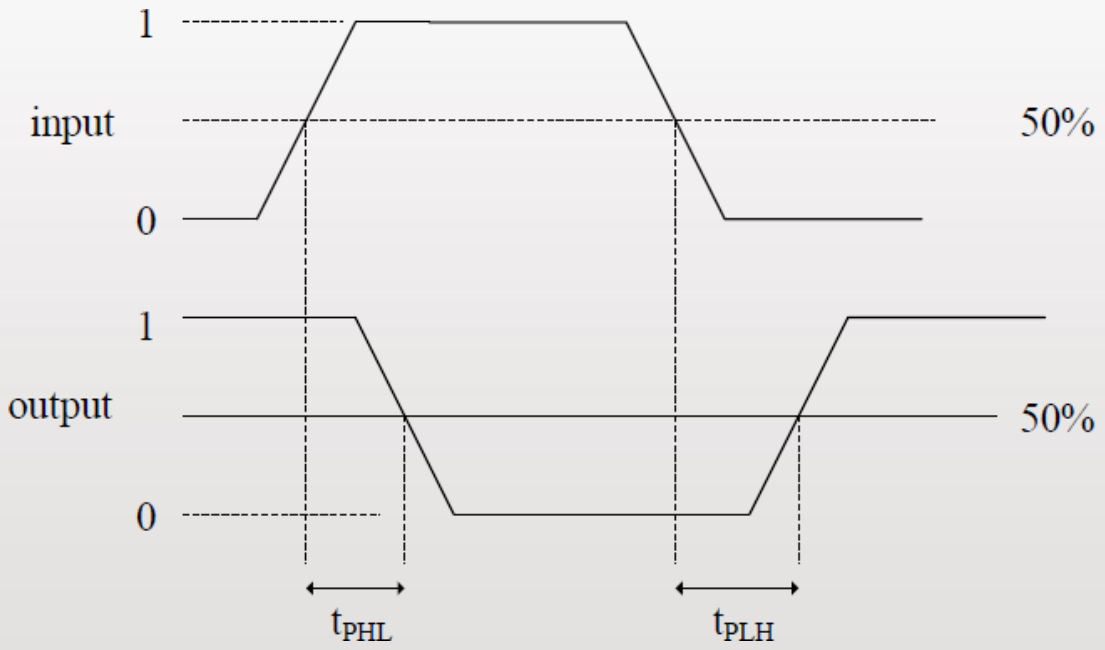




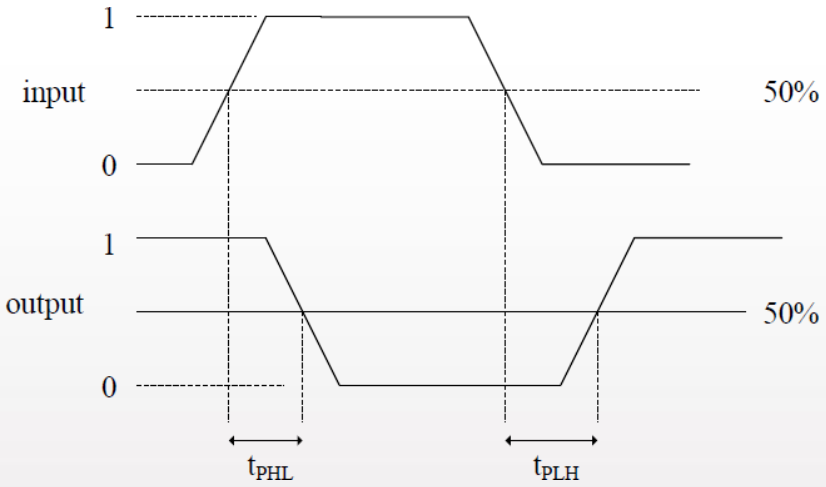
Propagation Delay

- Logic outputs need time to change from 0 to 1 or 1 to 0.
- Propagation delay is measured at 50%





Propagation Delay



$$t_P = \frac{t_{PHL} + t_{PLH}}{2}$$

t_{PHL} = time between input change and output changing from HIGH to LOW

t_{PLH} = time between input change and output changing from LOW to HIGH

TTL Power Dissipation

$$P_D = V_{CC} \times I_{AVE}$$

$$I_{AVE} = (I_{CCH} + I_{CCL})/2$$

where

V_{CC} = supply voltage

I_{AVE} = average current

I_{CCH} = current in HIGH state

I_{CCL} = current in LOW state

Power Dissipation

$$P_D = C_L \times (V_{DD}^2/2) \times f$$

where

V_{DD} = supply voltage

C_L = load capacitance

f = switching frequency

Power dissipation is dependent on switching activity

Power is dissipated only on 0→1 transitions

Noise Immunity

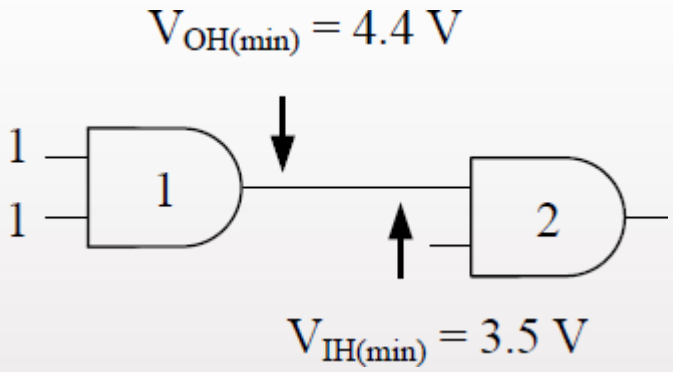
- Noise
  - unwanted signal in electrical circuits caused by electromagnetic radiation or power transmission lines
- Noise margin
  - A measure of a circuit's ability to tolerate a certain amount of noise

Noise Immunity

- V_{NH} = high level noise margin

  $V_{OH(min)} - V_{IH(min)}$
- VNL = low level noise margin

  $V_{IL(max)} - V_{OL(min)}$
- Example for 5V CMOS
- $V_{NH} = 4.4V - 3.5V = 0.9V$



Fan-out

- Fan-out is the maximum number of load gate inputs that can be connected without adversely affecting the specific operational characteristics of a gate.
- If a gate has a fan-out of 10, then it can drive 10 other similar gates.
- We use the lower of two fan-outs, LOW and HIGH

$$\text{Fan-out}_{LOW} = I_{OL}(max)/I_{IL}(max)$$
$$\text{Fan-out}_{HIGH} = I_{OH}(max)/I_{IH}(max)$$
$$\text{Fan-out} = \min(\text{fan-out}_{LOW}, \text{fan-out}_{HIGH})$$

Thank You!

Helang Ekor Cabang / Black Kite / Milvus migrans di Kuala Gula, Perak