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ONLINE LEARNING

Digital Electronics (SKEE1223)

Standard Combinational Circuits I

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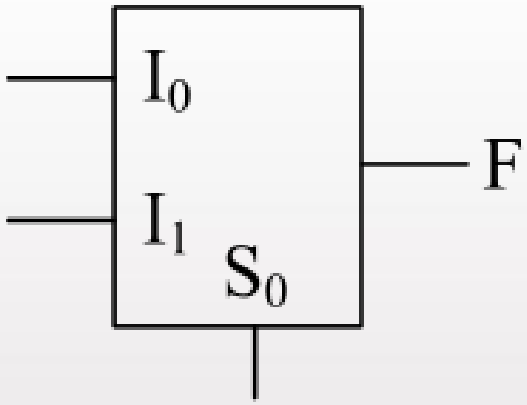
Classification of Integrated Circuits

IC Types	Acronym	Number of Gates	Types of Circuits
SSI	Small Scale Integration	<12 gates	Basic gates
MSI	Medium Scale Integration	12-99 gates	Encoder, decoder, counter, register, multiplexer, arithmetic circuit, small-sized memory
LSI	Large Scale Integration	100-999 gates	Processor, medium-sized memory, programmable logic device
VLSI	Very Large Scale Integration	>1000 gates	Microprocessor, large-sized memory

Multiplexers

- Circuits with many inputs and one output.
- At any one particular time, only data to a particular input can be sent to the output. This is done by using the control or select bits.
- Also called data selector
- Usually shortened to MUX

2-to-1 Multiplexer

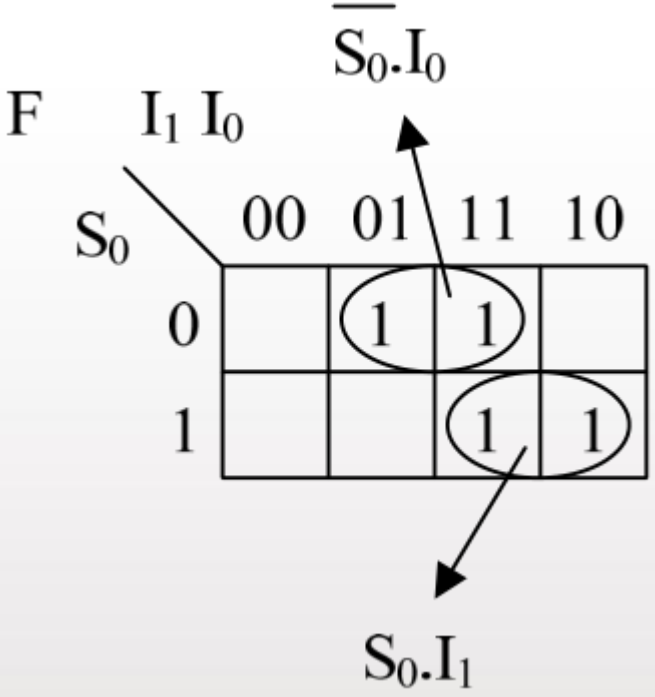


Logic symbol.

S_0	F
0	I_0
1	I_1

Function table.

2-to-1 Multiplexer



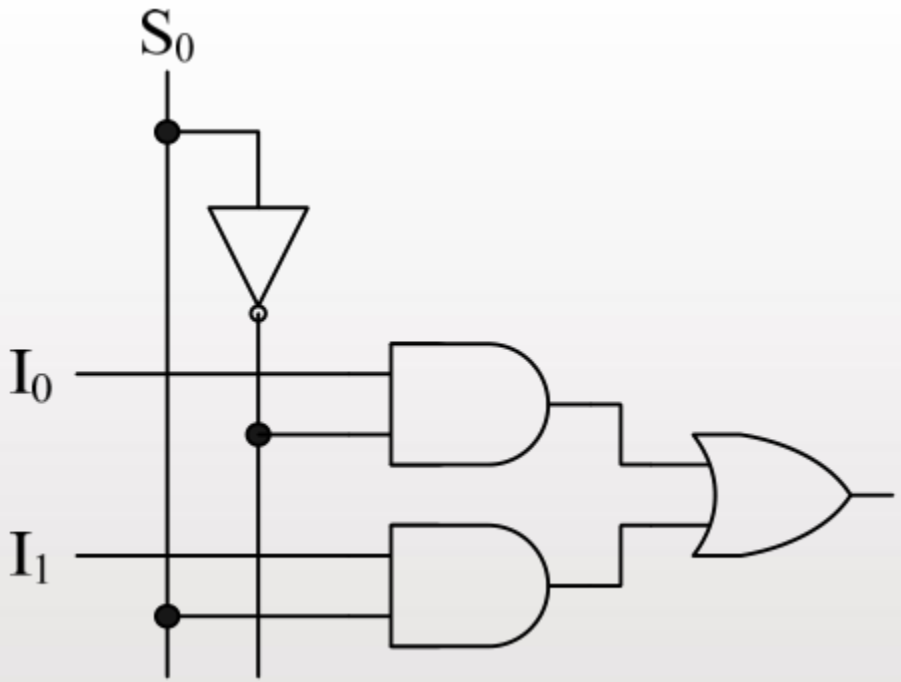
$$F = \overline{S}_0 I_0 + S_0 I_1$$

Equation

S_0	I_1	I_0	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

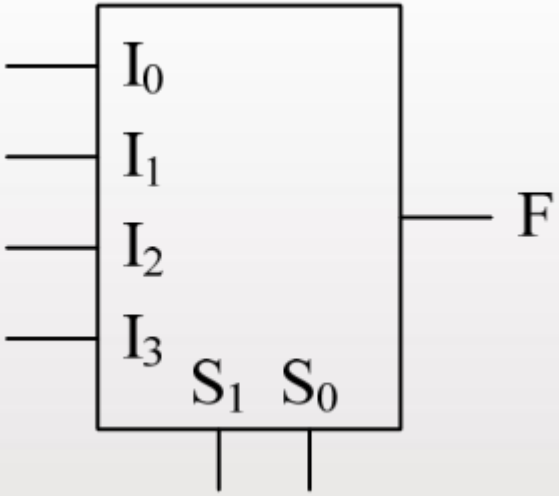
Truth table.

2-to-1 Multiplexer



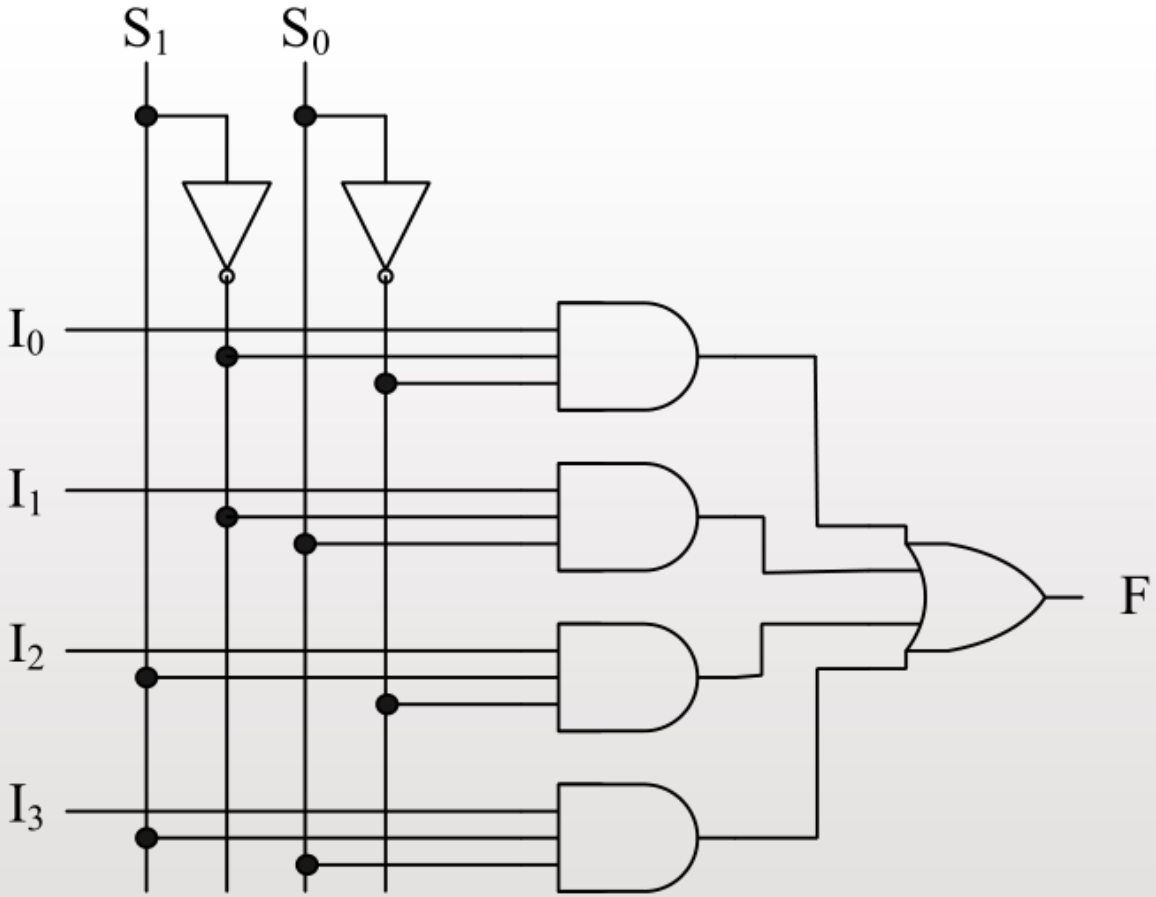
$$F = \bar{S}_0 I_0 + S_0 I_1$$

4-to-1 multiplexer

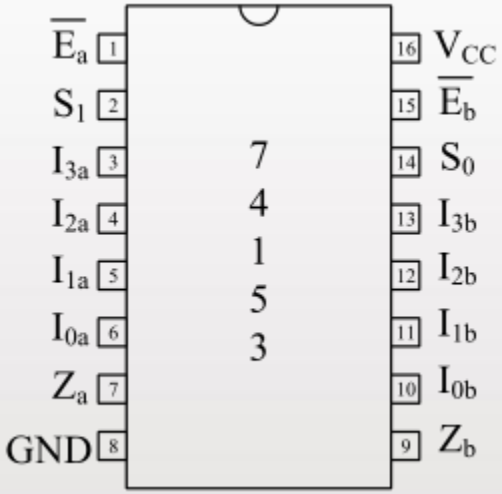


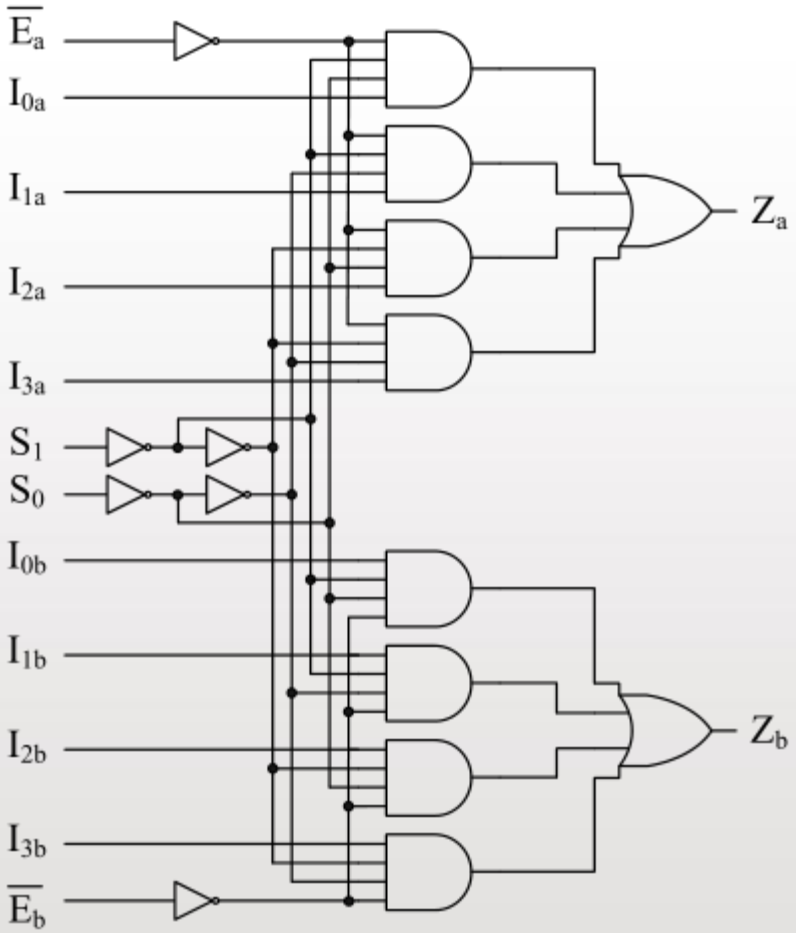
S_1	S_0	F
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

4-to-1 multiplexer

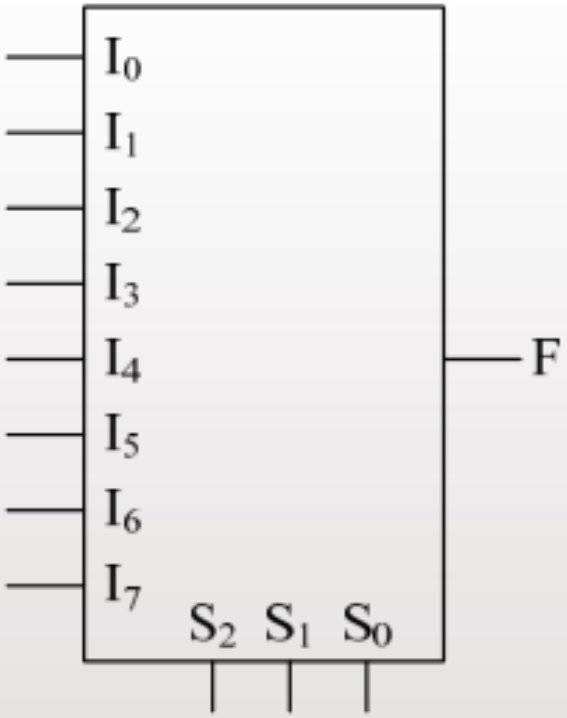


74153 Device



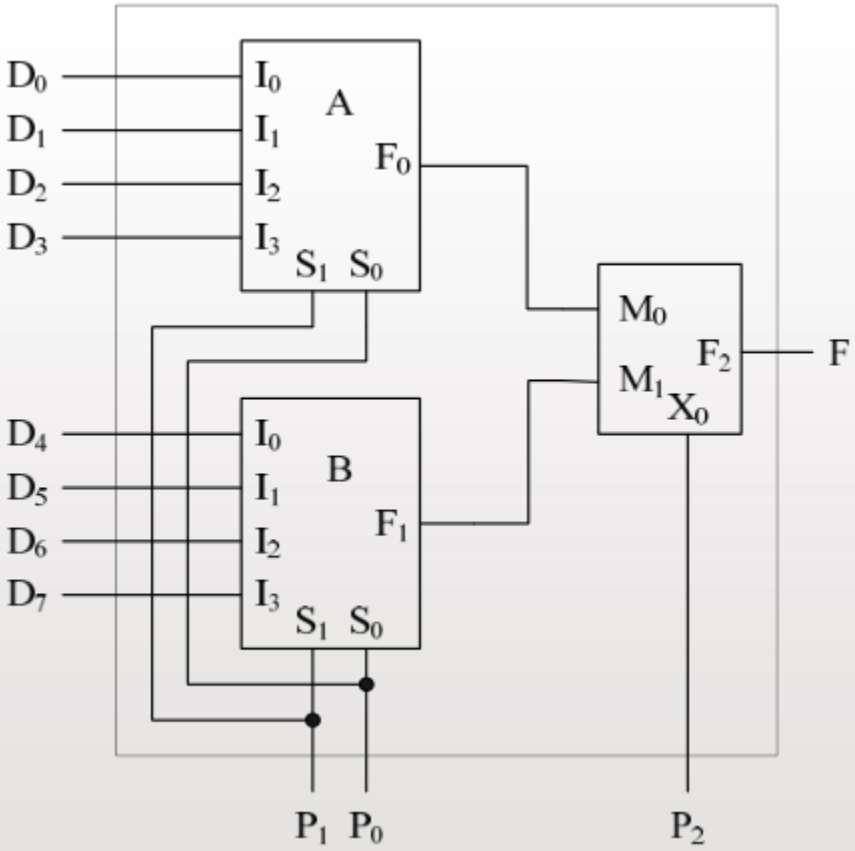


8-to-1 Multiplexer



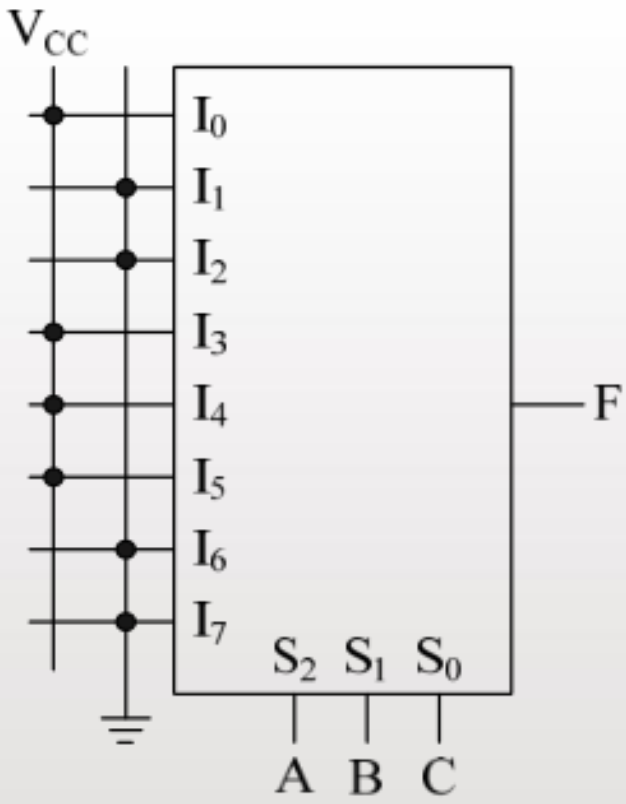
S_2	S_1	S_0	F
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

Multiplexer Expansion



Implementing Boolean Functions

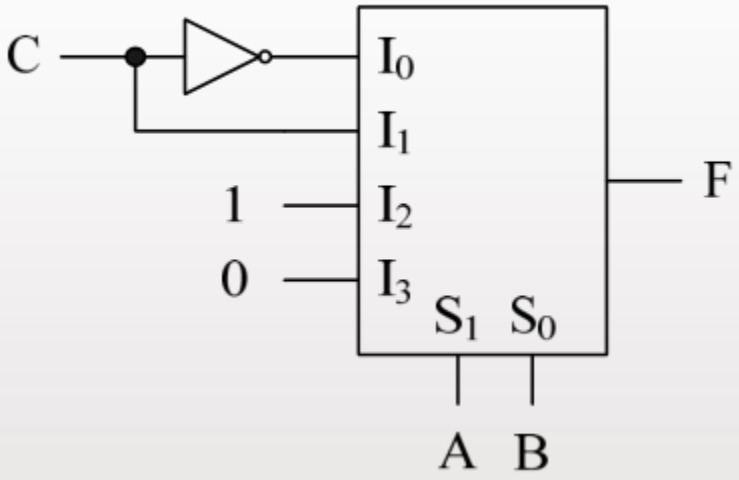
A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0



Implementing Boolean Functions

A	B	C	F	
0	0	0	1	$\bar{C}$
0	0	1	0	
0	1	0	0	C
0	1	1	1	
1	0	0	1	1
1	0	1	1	
1	1	0	0	0
1	1	1	0	

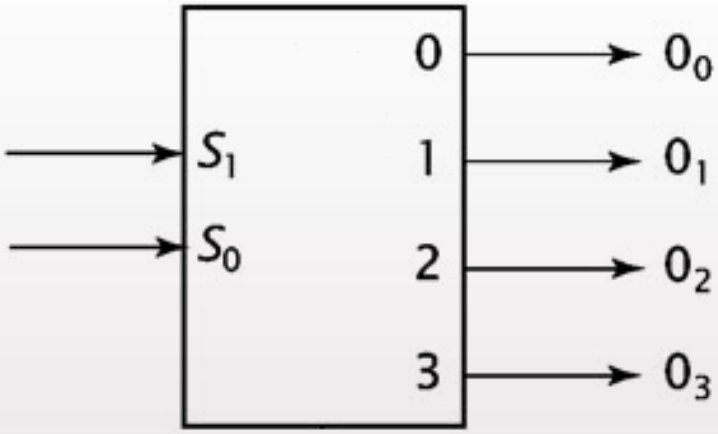
A	B	F
0	0	$\bar{C}$
0	1	C
1	0	1
1	1	0



Decoders

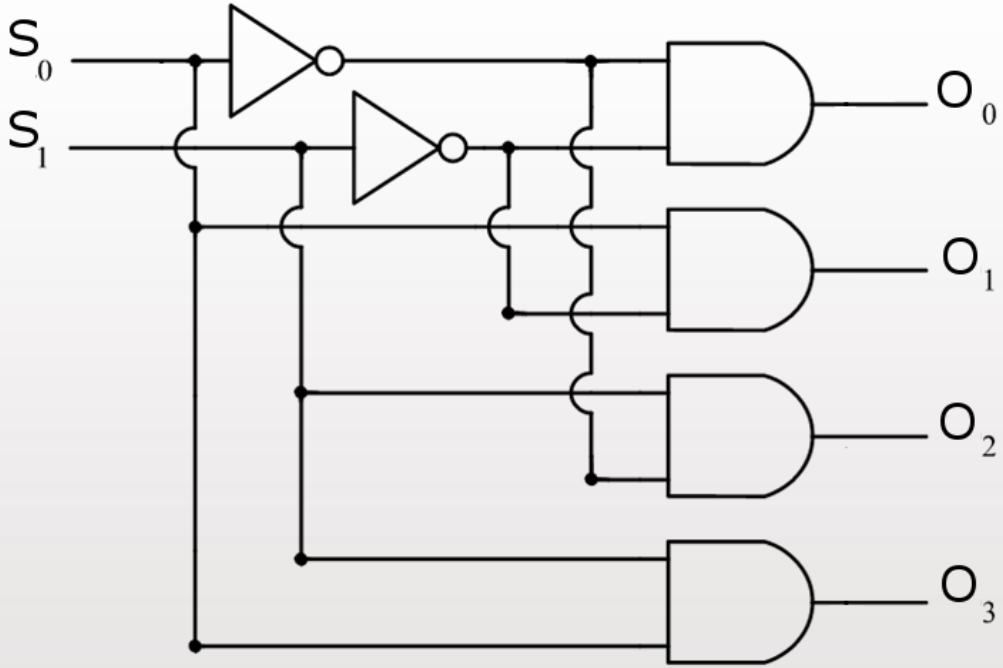
- A circuit that converts binary information from *n* input lines to a maximum of 2^n unique output lines
- If the original bit pattern is a code, the decoder undoes the encoding so that the original information can be retrieved

2-to-4 Decoder



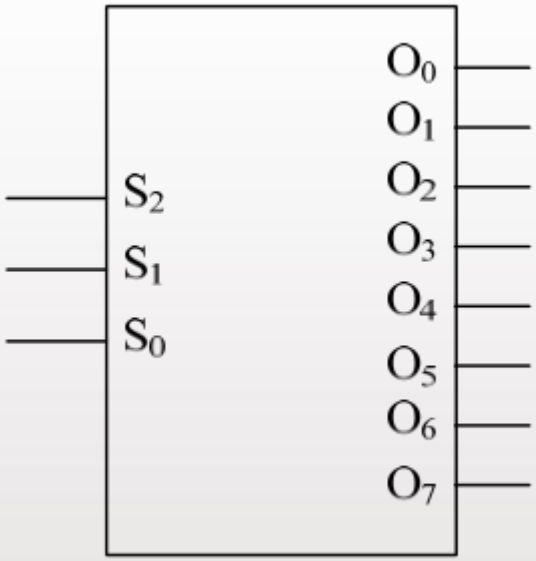
S_1	S_0	O_0	O_1	O_2	O_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

2-to-4 Decoder



$$O_0 = \overline{S}_1 . \overline{S}_0$$
$$O_1 = \overline{S}_1 . S_0$$
$$O_2 = S_1 . \overline{S}_0$$
$$O_3 = S_1 . S_0$$

3-to-8 Decoder

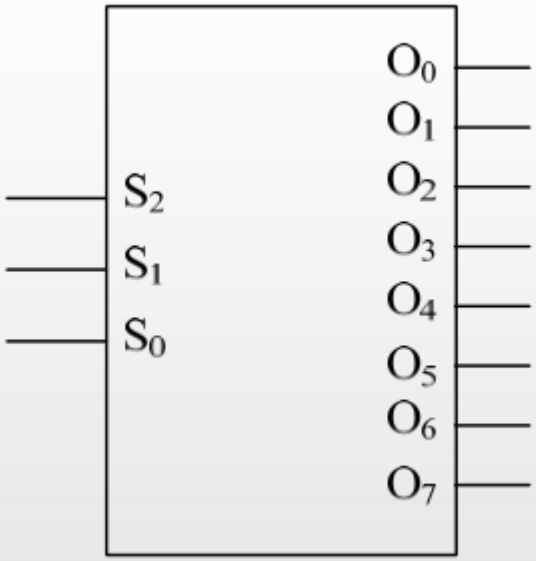


$O_0 = \overline{S_2}.\overline{S_1}.\overline{S_0}$ $O_1 = \overline{S_2}.\overline{S_1}.S_0$ $O_2 = \overline{S_2}.S_1.\overline{S_0}$

$O_3 = \overline{S_2}.S_1.S_0$ $O_4 = S_2.\overline{S_1}.\overline{S_0}$ $O_5 = S_2.\overline{S_1}.S_0$

$O_6 = S_2.S_1.\overline{S_0}$ $O_7 = S_2.S_1.S_0$

3-to-8 Decoder

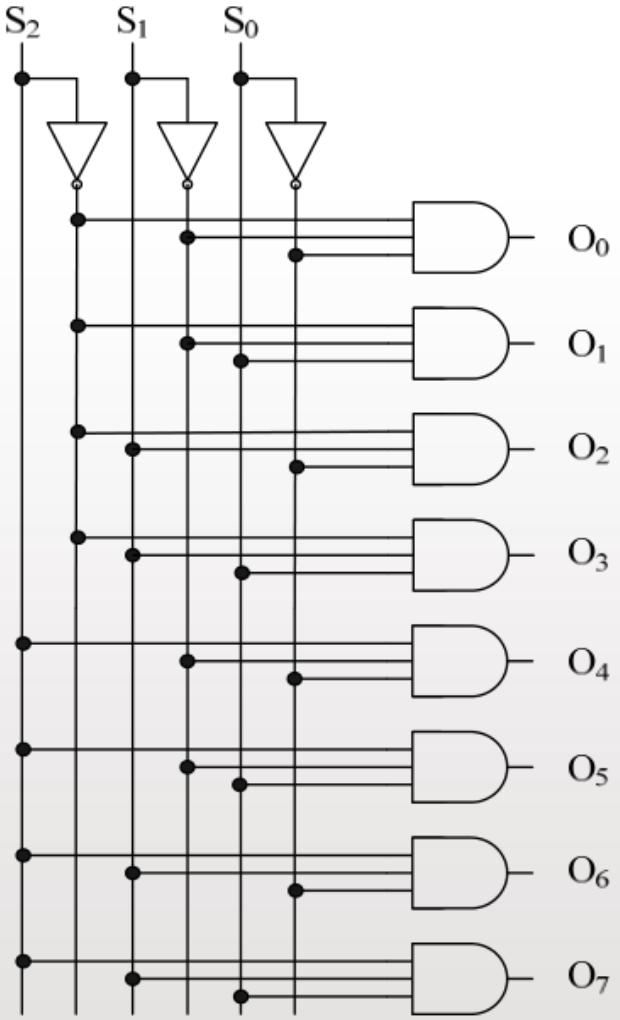


$O_0 = \overline{S_2}.\overline{S_1}.\overline{S_0}$ $O_1 = \overline{S_2}.\overline{S_1}.S_0$ $O_2 = \overline{S_2}.S_1.\overline{S_0}$

$O_3 = \overline{S_2}.S_1.S_0$ $O_4 = S_2.\overline{S_1}.\overline{S_0}$ $O_5 = S_2.\overline{S_1}.S_0$

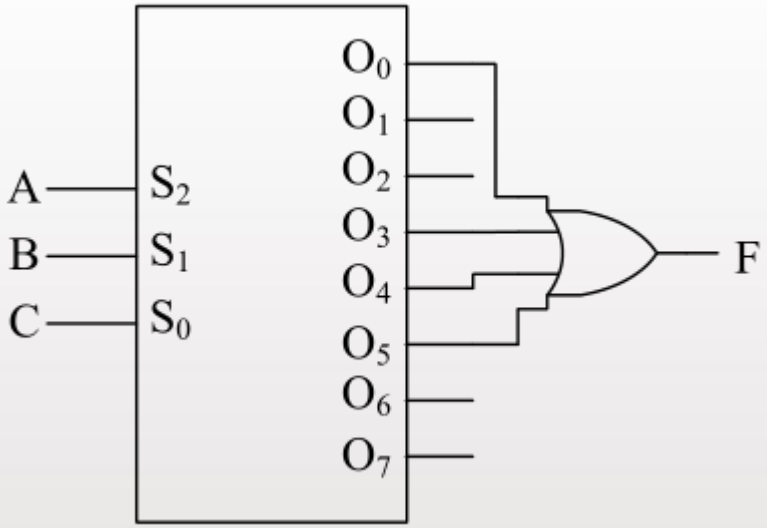
$O_6 = S_2.S_1.\overline{S_0}$ $O_7 = S_2.S_1.S_0$

S_2	S_1	S_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

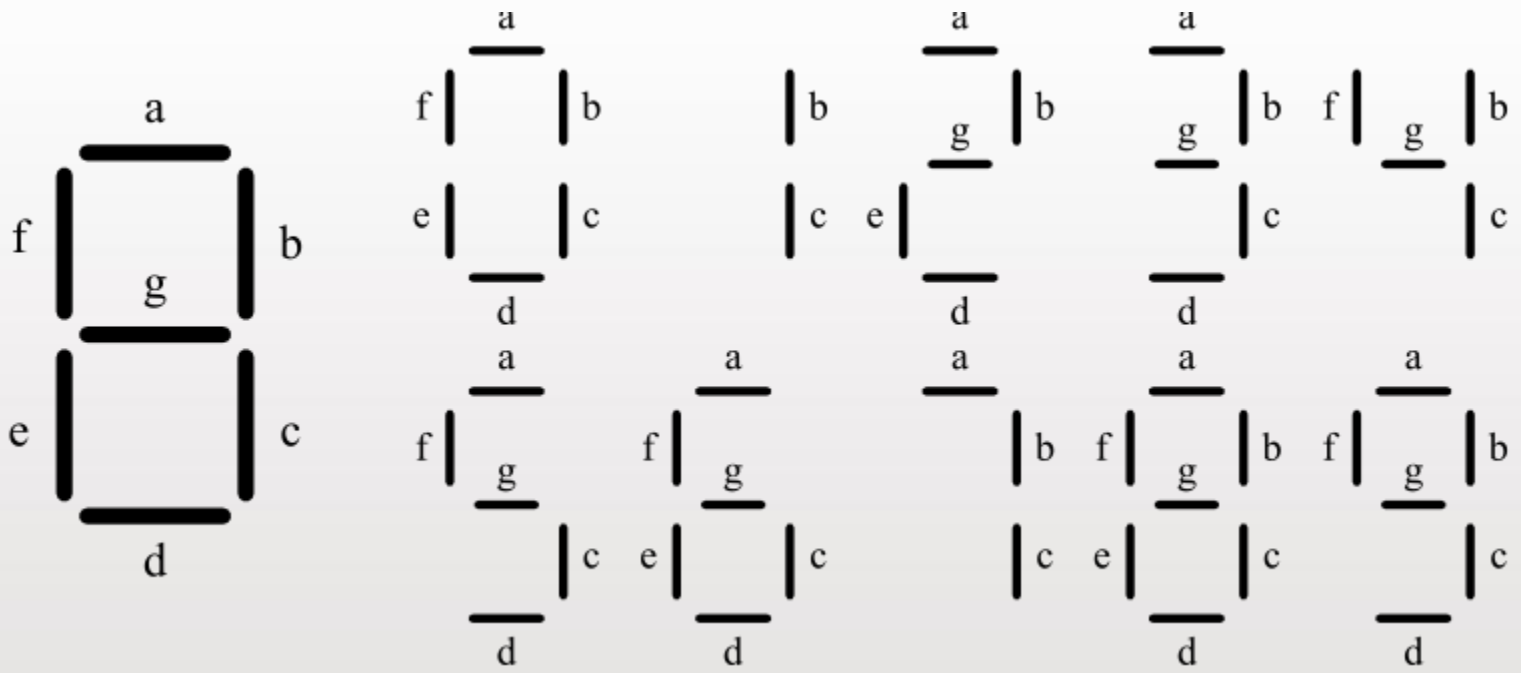


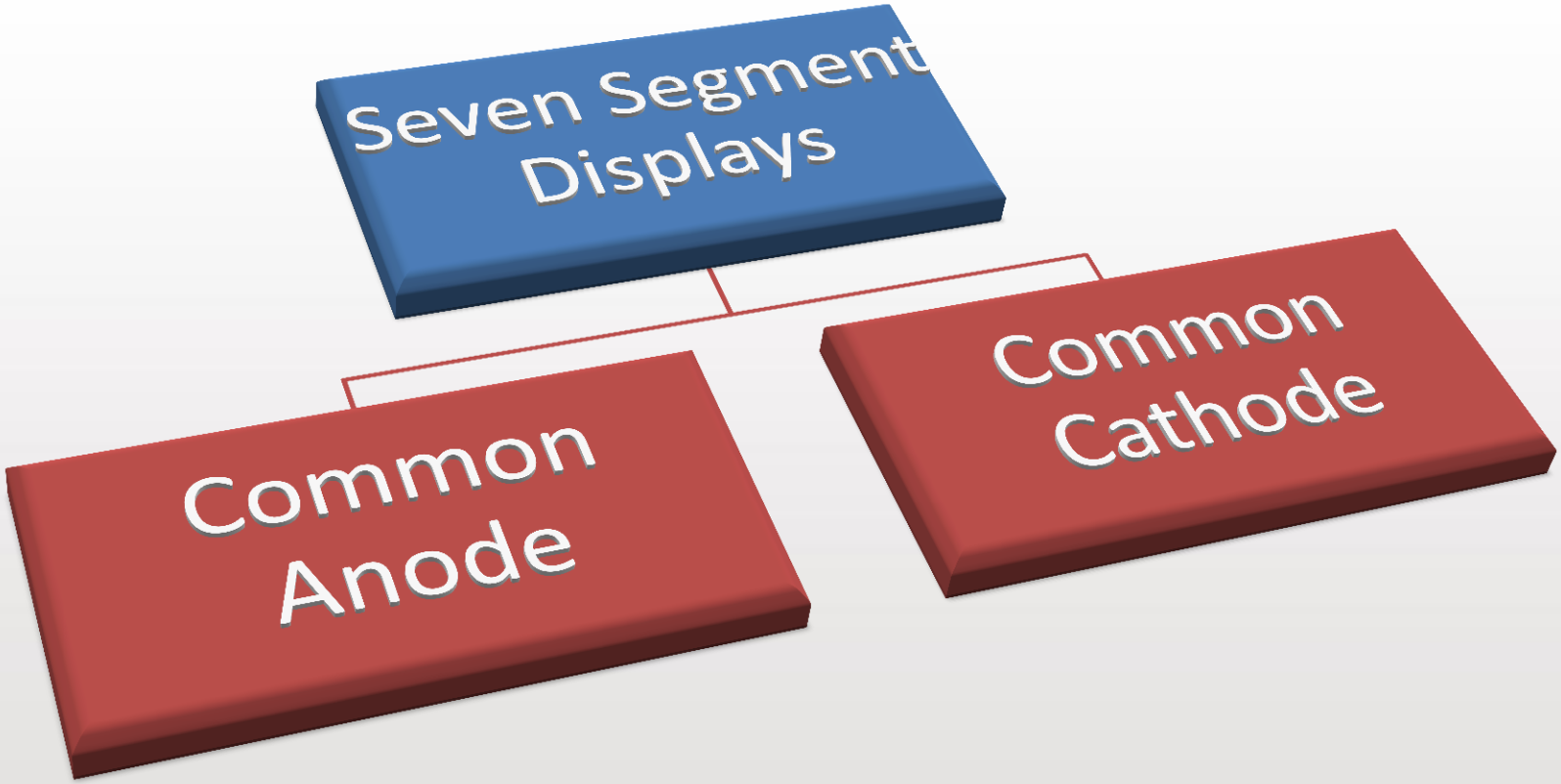
Implementing Boolean Functions

A	B	C	F	
0	0	0	1	O_0 or $\overline{O_0}$
0	0	1	0	O_1 or $\overline{O_1}$
0	1	0	0	O_2 or $\overline{O_2}$
0	1	1	1	O_3 or $\overline{O_3}$
1	0	0	1	O_4 or $\overline{O_4}$
1	0	1	1	O_5 or $\overline{O_5}$
1	1	0	0	O_6 or $\overline{O_6}$
1	1	1	0	O_7 or $\overline{O_7}$

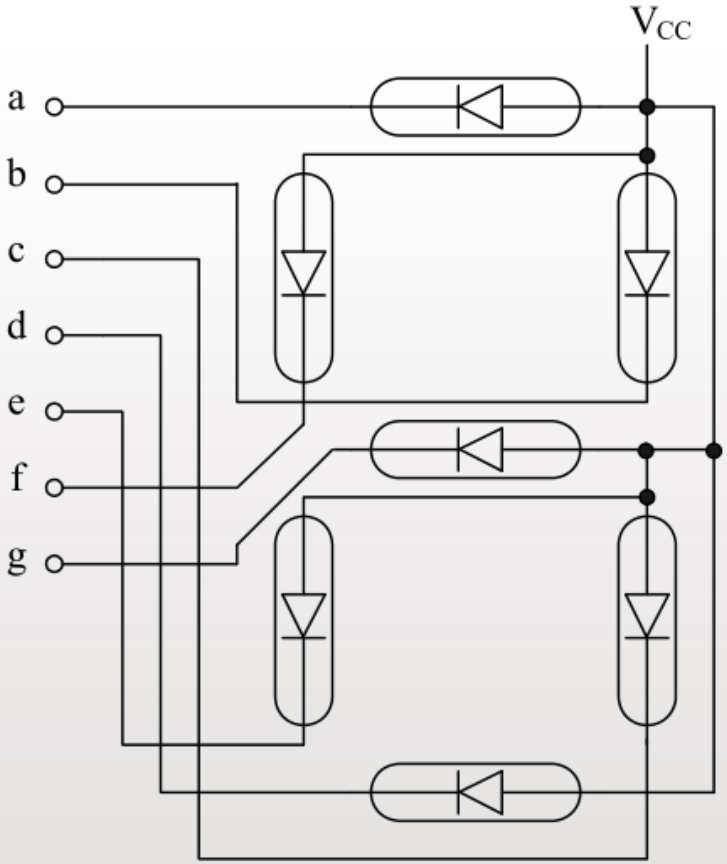


BCD to Seven Segment Display Decoder

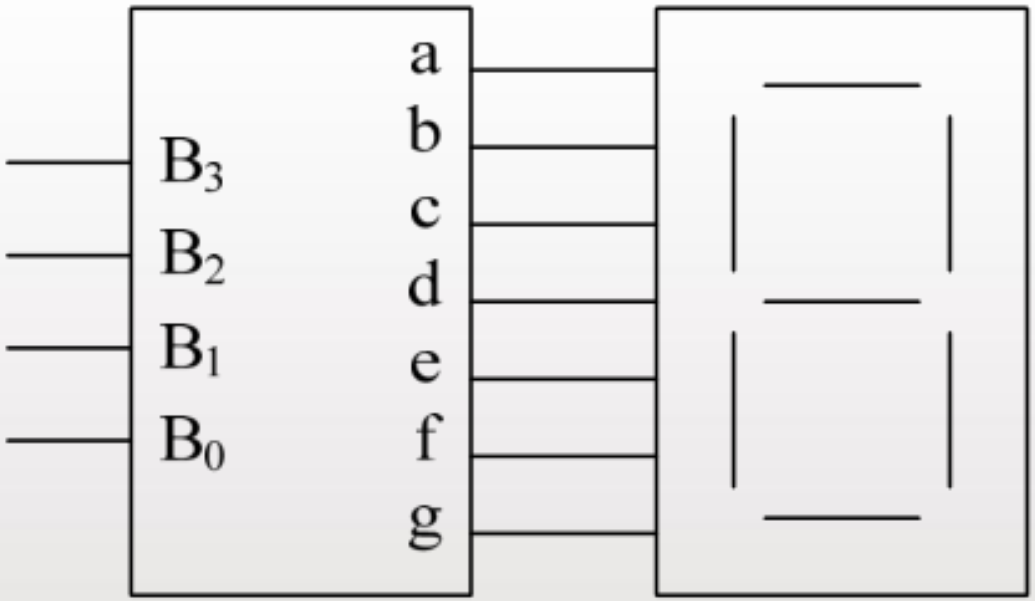



Seven Segment Displays
Common Anode
Common Cathode

Common Anode LED Display



Decoder to Display Connection



BCD decoder 7-segment display

Decoder Truth Table (for common-cathode display)

B_3	B_2	B_1	B_0	*a*	*b*	*c*	*d*	*e*	*f*	*g*
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1