

SET 4573: Data Communication and Switching System

Chapter 3: Data Communication Basic

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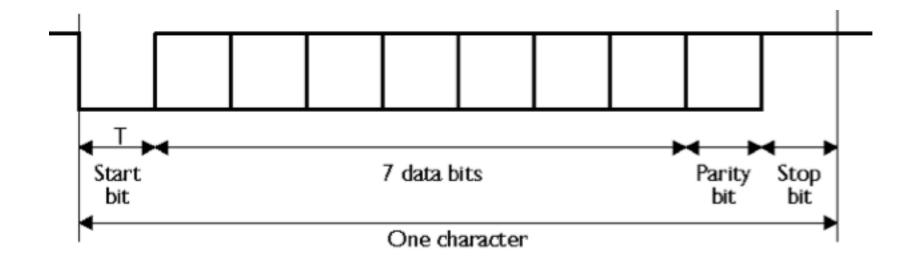
Asynchronous and Synchronous Transmission

- Synchronization is to synchronize the transmitter and receiver
 - receiver samples data stream at bit intervals
 - the clocks has to be aligned so that the sampling is done at the correct time
- Two solutions to synchronizing clocks
 - asynchronous transmission
 - synchronous transmission



Asynchronous Transmission

- Simple and cheap method of transmission
- Every character is sent with overhead of 2 or 3 bits (start, parity and stop bit)
- ~20% loss due to overhead





Synchronous Transmission

- block of data transmitted sent as a frame/packet
- clocks must be synchronized
 - using separate clock line or
 - embedded clock signal in the data sent
- indication for the start and end of block
 - use preamble and postamble (flag and control fields)
- more efficient (lower overhead) than asynchronous transmission

| 8-bit | Control | Data Field | Control | 8-bit |
|-------|---------|------------|---------|-------|
| flag | fields | | fields | flag |



Error in Transmission

- an error occurs when a bit is altered between transmission and reception process
 - e.g. from '1' to '0' or vice versa
- single bit errors
 - only one bit altered
- burst errors
 - sequence of several bits in error
 - mostly occur at higher data rates



Error Detection

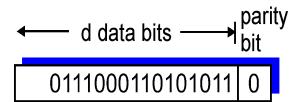
- detect using error-detecting code
- added by transmitter
- recalculated and checked by receiver
- example
 - parity
 - parity bit is set so character has even (even parity) or odd (odd parity) number of '1'
 - even number of bit errors cannot be detected
 - Cyclic Redundancy Check (CRC)
 - check a block number of bits



Parity Checking

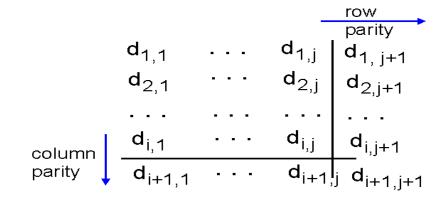
Single bit parity:

Detect single bit error



Two Dimensional Bit Parity:

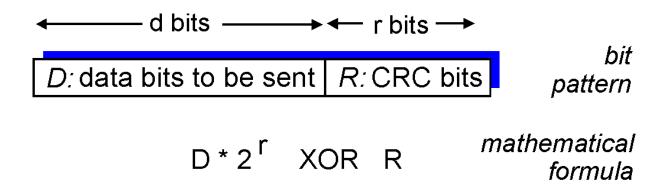
Detect & correct single bit error





Cyclic Redundancy Check

- for a block of d bits, transmitter generates an r bit of CRC bit
- transmits (d+r) bits which is exactly divisible by a predetermined number, G (r+1) bits
- receiver divides the frame by G (modulo 2)
 - if no remainder, no error detected



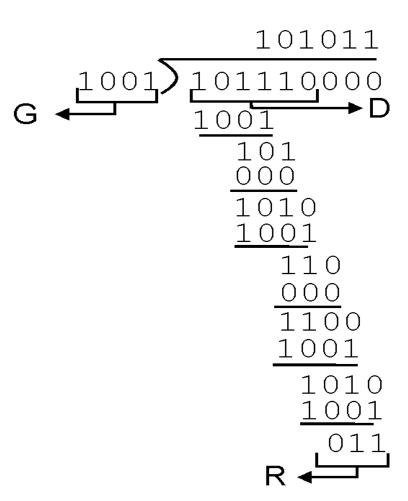


CRC Example

Divide D·2^r by G using modulo-2

Add the remainder R to the end of the bits

$$R = remainder[\frac{D \cdot 2^r}{G}]$$





Error Control

- Detection and correction of errors
- 2 types of 'error'
 - lost frames
 - damaged frames
- Error correction
 - positive/negative acknowledgment
 - retransmission
 - after timeout
 - if negative acknowledgement



Flow Control techniques

- Stop and Wait
- Sliding Window
 - Go-back-N
 - Selective Reject



Stop and Wait

- Source transmits single frame/packet
 - wait for ACK for the frame sent
 - if ACK frame received correctly, send the next frame
 - if negative ACK frame is received, retransmit the sent frame
 - if no ACK frame received within timeout,
 retransmit the sent frame



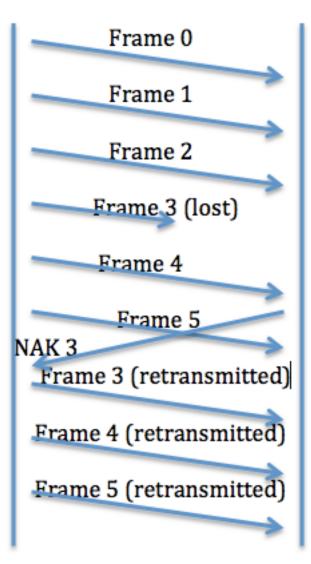
Go-Back-N

- Works based on sliding window
 - send multiple number of frame simultaneously
 - the number of frames that can be sent depends on window size
 - one ACK frame can acknowledge a number of frames sent
- If negative ACK is received for a frame
 - retransmit the 'error frame(s)' and all subsequent frame(s) that have been sent



Go-Back-N Diagram

A F





Selective Reject

- Almost the same with go-back-N
 - only rejected (error) frames are retransmitted
 - subsequent frames are accepted by the receiver and buffered and will not be retransmitted
- Minimizes retransmission
 - retransmit only the 'error/corrupted frame(s)'
- Receiver must maintain large enough buffer to store already sent frame(s)



Selective Reject-Diagram

